資　料

第5回日独情報技術フォーラム
会　議　録

期　間：　昭和63年11月24日〜26日

会　場：　国立京都国際会館

平成元年3月

目　　次

1. 日独情報技術フォーラム趣旨

1. 日独情報技術フォーラム趣旨

　日独情報技術フォーラムは，高い技術レベルと経済力を有するドイツ連邦共和国とわが国が，情報技術分野における両国の相互理解と交流を一層深め，活発な産業，技術協力の展開を通じて世界の情報化に寄与していくことを目的に1983年8月ドイツ連邦共和国研究技術省のハインツ・リーゼンフーバー（Dr.Heinz Riesenhuber）大臣と当時の宇野宗佑通商産業大臣との間で，その設置が合意されたものである。当該フォーラムは，両国の情報技術に関わる産業分野，学術分野，及び行政分野の指導的立場にある人々が一堂に会し，両国の研究開発のあり方，協力のあり方等について幅広い意見交換を行うと同時に，人的交流を深めることをねらいとしている。

　当フォーラムは，毎年一回両国で交互に開かれることになっており，84年4月には第1回が東京で，85年4月には第2回がベルリンで，86年10月には第3回が東京で，87年10月には第4回がシュツットガルトで，それぞれ開催されている。

2. 開 会 挨 拶

2. 開 会 挨 拶

2.1 本田幸雄 通商産業省機械情報産業局電子機器課長

　皆様，おはようございます。ご紹介頂きました通商産業省機械情報産業局電子機器課長の本田でございます。本日ここに第5回日独情報技術フォーラムが開催されることに当たりまして，通商産業省を代表致しまして一言ご挨拶を申し上げます。

　わが国の情報化は，本格化して以来約4半世紀を経ておりますが，近年の技術革新に伴いネットワーク化を進めながら，産業，社会，家庭生活の各分野において，広くかつ深く浸透しつつあります。また，情報化は地域社会の中にも点から線，線から面へと急速にその輪を広げ，経済活動において，非常に重要な役割を果たしつつあります。

　しかしながら，高度情報化社会の実現に向けていまだ種々の問題が山積みされており，これらの課題への的確な対応が急務とされております。こうした認識のもとで，通商産業省といたしましては，情報化社会を底辺から支える情報処理技術者等の人材育成や，情報化教育の充実，ソフトウェアの量的・質的不足への対応，データベースの整備，多種多様な情報関連機器システムの相互運用性の確保，情報関連技術開発の一層の推進等を通じて，情報化基盤の整備及び情報化の推進の為，人材，ソフトウェア，ハードウェア，データベースの各方面から総合的な情報関連施策を展開しておるところでございます。

　しかしながら，近年の情報化は国際的通信回線を用いたトランザクション処理等に見られますように，国境を越えた情報の流通を促しております。また，ISOの場を中心にしたOSIプロトコルの審議，策定等にみられますように，今や国際的な協調ぬきには情報化を語ることはできません。その意味で，当省といたしましても，本フォーラムを積極的に推進しておるところでございます。

　日独関係を振り返ってみますと，わが国はドイツ連邦共和国から医学，土木，機械などの分野において，多くの科学技術を導入いたしました。わが国の東半分の地域で使われている電気が50ヘルツなのは，最初にドイツから導入した発電機が50ヘルツだったためであります。また，戦後ではロータリーエンジンの技術がドイツ

連邦共和国から導入され，わが国で開花致しました。

　近年では貿易，投資交流の面で，ドイツ連邦共和国とわが国とは，緊密な関係を維持しております。自動車，医療機器，コンピュータ等の工業製品を中心とする両国間の貿易は，ここ数年一貫して増加しています。ドイツ連邦共和国の11の州政府のうちの大半が対ドイツ連邦共和国投資の誘致の為の駐日事務所をわが国に設置されているのは，意外と知られていない事実でございます。

　研究交流の面でも，1974年に締結されました科学技術協力協定のもとで広範な技術分野の研究協力が着実に実施されております。その一環で，1985年からドイツ連邦共和国の物理工学研究所と当方の計量研究所，1986年からドイツ連邦共和国の航空宇宙研究所と九州工業技術試験所との間で，それぞれ高安定レーザーを用心た超高感度センシング技術に関する研究と，耐熱性炭素セラミックスの開発とその高温特性に関する研究を，国際特定共同研究事業として実施しております。

　また，科学技術協定以外にもドイツ連邦共和国のスペースラブD２計画にわが国の企業が参加しております。このように，研究交流の面を含め経済面全般において，ドイツ連邦共和国とわが国との間の協力関係が深まりつつあることは喜ばしいかぎりでございます。

　国際的な情報化の進展，また，先進国間の多面的な協調の必要性を考える時，当フォーラムの日独双方にとっての意義，重要性は従来にも増して大きなものになって来つつあります。

　最後に本日から２日半にわたって開催されます当フォーラムが日独両国の研究交流に資する事を，ひいては日独関係の発展に寄与することを祈念致しまして，私のご挨拶にかえたいと思います。

2.2　ギュンター・マークス　研究技術省情報処理担当課長

　皆様，おはようございます。まず，日本側関係者の皆様方に，この第５回日独情報技術フォーラムへのご尽力及び私共をお呼びいただきましたことに対しましてお礼を申し上げます。

　ドイツ連邦共和国と日本は，盛んな輸出と高度な技術力を有する国といたしまし

て，知識と経験を交換する必要性にかられております。そのためには両国政府によって開催されますフォーラムが大変に重要な役割をはたすものでありましょう。

情報技術と言いますのは，テクノロジーの各分野の中におきましても，とりわけ急速な進歩を遂げているという特徴を持っています。この分野で成功をおさめようとするなら，常に目を未来に向けまして，その発展の本質的な傾向をいち早く，早期につかむことが必要でございます。

なぜドイツ連邦共和国政府が情報技術に特に注目しているかと申しますと，その理由としましては，この技術の持ちますその強力な広範囲に及ぼす効果でございます。情報技術こそ，非常に広大なスケールによる製造及びサービスの基盤となるものでありまして，これなくしては，そのような製造もサービスも考えられない，あるいは競合力を持ち得ないものでありましょう。

この重要なポイントによって，情報技術は高度にランク付けされるテクノロジーとなっております。そして，産業と学術との協力体制及び国際的な方向性とを促しているのでございます。

ドイツと日本の企業は，市場におきましては競合相手でありまして，従って両者が１つのテーブルに同席して意見を交換するということはそれ程簡単なことではございませんでした。

しかしながら，国境を越えての協力と意見の交換があってこそ，今後の課題に打ち勝っていけるのです。それ故に両国政府が５年前にこのフォーラムを設置する運びとなりました。

これは１つの実験であったわけでございますが，成功した実験であると確信しております。産業と学術の専門家間のコンタクトが得られました事によって，両国政府の当面の目標はとりあえず達成されたわけでございますので，それ故に今回のフォーラムでは私達は，今後の協力体制がどのようにあるべきかについても考えていく必要があると思います。

私達は，この第５回日独情報技術フォーラムにおきましては，ニューメディア，コンピュータ，半導体の分野での発展に関してのディスカッションを予定しております。これらの情報技術の核を成します本質的な分野でございます。参加者のリス

トを拝見させて頂きましても，情報技術の未来についての私達のイメージをより豊かにしてくれるような，実り多い示唆に富んだディスカッションが期待できるものと存じます。

では最後に第5回日独情報技術フォーラムが実り多く，成功裡に終わります事を願いまして挨拶とさせていただきます。どうもありがとうございました。

2.3　柳井久義　日本側議長　芝浦工業大学学長

皆様，おはようございます。今回の第5回日独情報技術フォーラムは日本におきまして，ここ京都で開催されることになりましたため，ドイツ側議長のエングル先生も多分日本語でご挨拶なさるようですので，私も日本語で挨拶させていただきます。

今回の第5回日独情報技術フォーラムが，この古都，京都で開かれることになりましたことを，たいへん嬉しく存じます。今回の日独情報技術フォーラムは第5回ということでございまして，過去4回のフォーラムでは参加者の皆様方のご協力によりましてお互いの研究，あるいは産業の状況というものや，情報技術に関しての状況というものを，たいへんよく理解し合えたのではなかろうかと思います。

第5回になりますので先ほどドクター・マークスがおっしゃいましたように，今後のあり方についても更に検討を要すると思いますが，今回はさらに情報の交換を深めるという意味において，従来同様に実りあるディスカッションが行われますことを期待しております。

それでは皆様，実りあるディスカッションを通して，仕事の面で大きな成果を挙げていただきますと共に，また，この京都で，京都の秋を十分享受していただきたいと思います。どうもありがとうございました。

2.4 ワルター・L・エングル ドイツ側議長 アーヘン工科大学教授

皆様，1984年に情報技術における第1回日独情報技術フォーラムが東京で開催されました。「討論会」の語源はラテン語のフォラムでありました。この単語は，「主会場」という意味です。このような自由意見の交換が行える，年に1度のフォーラムに発展することを確信する親しい友人達により出現したものであります。

今回は第5回目を迎え，このようなよい結果を得るに当たってご協力いただいた方々に感謝しております。特に今までの日本側の議長であられた3名の方のお名前を申し上げておきたいと思います。今は亡き元岡達教授，そしてやはり亡くなられた宮川洋教授，そして現在新しい責務に挑んでいらっしゃる田中昭二教授です。

我々は変な社会に生きています。この社会はハイテクノロジーの恩恵を十分享受しているにもかかわらず，最新の技術進歩に対し反対または少なくとも恐れを感じています。高度技術革新により，ますます競争が激しくなってきている今日でありますが，これがなければ最新の技術が前進することはありえないでしょう。ただし，この場合でも協調し合う環境は重要であり，競争意識と矛盾してはならないと思います。

5年間でお互いの立場を理解し自由なアイデアを交換し，さらに友好を深めることが出来るようになったと感じます。しかしまだ改良の余地があります。今回皆様にお集まりいただいた目的の1つでもあると思います。このフォーラムは初めて京都で開かれましたのでドイツのご参加の方々へ少し話をさせていただきたいと存じます。

東京が外の世界の方を向いているのに対し，京都は未だに日本の源泉を見つめています。ですから，どうかこの機会を使って，昨日，奈良に行きましたように，京都の持つ文化遺産を訪ねるようではありませんか。皆さんの瞳を京美人の風情で楽しませ，皆さんの舌には京料理を味あわせましょう。1つだけ皆さんにお奨めしたいことがございます。真の学者魂の求めるままに冒険心を持ちなさい。観光客が通る路からはずれれば，何百という隠れた神社仏閣が静けさの中であなたを待ち，抱擁してくれるでしょう。そして，そこで平静を見いだしさらなる勤労の1年にそなえる力を取り戻しなさい。

今回の第5回日独情報技術フォーラムが両国の科学及び産業界の協調に貢献することを期待しております。ありがとうございました。

柳井議長よりエングル議長の挨拶へのコメント

　ちょっと合いの手を入れさせていただきます。ただ今エングル先生が日本語でお話になりましたが，一部の方はよくご存じだと思いますけれども日本の参加者のまだご存じない方もあろうかと思いますので，今もちろん原稿をお読みになったわけですが，その原稿は漢字及びカタカナで自分で書いておられます。そのことをご承知いただきたいと思いますのでちょっとご紹介しておきます。

3. 各分科会サマリー

3. 各分科会サマリー

3.1 ニューメディア分科会

〔ニューメディア分科会日本側主査　大越孝敬〕

　まず最初に，過去4回のフォーラムにおける主題と討論をふりかえってみたいと思います。1984年の東京での第1回フォーラム及び1985年のベルリンでの第2回フォーラムでは，主題はかなり広範で新しい情報メディアのあらゆる局面を網羅しておりました。それらの初期の会合では，私たちの主な目的がお互いをよりよく知り合うことにあったからであります。再度東京で開かれた第3回フォーラムでは，話題は狭くなりました。光学広帯域ネットワーク及びHDTVという2つの主題が選ばれました。

　昨年のシュットットガルトでの第4回フォーラムでは，主題はさらに狭められて，発表は過去の主題の1つであるHDTVと3次元テレビジョンの研究に絞られました。

　この京都会議の主題についての予備討論は，両国のコアメンバーの間で今年の4月に始まりました。ドイツと日本の間に多数のテレックスとテレファックスが往復した後に，今回は，現在強い関心のある4つの主な主題が含まれるように，話題の範囲を広げることが最終的に合意されました。それはここに示しましたように，広帯域ネットワーク及びISDN，光学スイッチ及び光学的信号処理，社会的アクセプタンス及びセキュリティ，並びにICカード，光カード及び，CD－ROMを含む新しい情報メディアであります。

　次に発表の順に従いまして，話題と討論についてご報告申し上げたいと存じます。

　木曜日の午後の第1セッションは，広帯域ネットワーク及びISDNが主題でした。東京大学の安田教授の最初の発表は，ビデオ送信の新しいコンセプトでるパケット形のビデオ送信機の説明でした。この計画ではビデオ情報が、パケット化されISDNまたは広域VAN，LANを通じてパケット形のメインシステムに送られます。この種の研究は，創始者の1人である安田教授を含め，世界中の多数の研究者によって現在極めて活発に行われています。

「Switching Concepts for Broadband ISDN」という表題の2番目の発表が，Siemens のシャッファー氏によって行われました。この表題は将来の広帯域ISDNにおける操作のATM（Asynchronous Transfer Mode）に関連したものでした。シャッファー氏は，このような新しいシステム技術の導入には「成長のシナリオ」とも呼ぶべきものが必要であることを強調されました。この種の大規模な社会的システムの改革には新旧システムの調和が必須であるからです。

　日本電信電話の江川氏による3番目の発表は，「日本におけるISDN」とい表題で，前の2つの発表とは違って既存の狭帯域ISDNを扱ったものでした。日本でのISDN開発計画の第1段階は，1980年に始まり1985年まで続きました。この期間に得られた経験を通して，日本はCCITT（国際電信電話諮問委員会）による標準化研究に貢献することができました。そして現在日本の多くのメーカがデジタル電話端末機，高性能ファックス機など種々のISDN端末機を生産しています。今年の9月現在で，日本全国で約 500名の加入者がISDNに参加しており，この数はいうまでもなく極めて急速に増加しています。

　つぎの発表は，「広帯域通信の導入の概念」という表題で，西ドイツ郵電省のシュタイナー氏が講演されました。シュタイナー氏は，社会での需要量が未知であるためネットワークの計画を立てることがかなり難しく，既存の社会に広域VANを導入するのが困難なことを述べられました。そのため，発展的な形の融通性のある開発計画が再度必要とされます。そのようなダイナミックな西ドイツ郵電省の開発計画が詳しく説明されました。

　つぎの5番目の発表では，ベルリンのHHIのハイト氏が，VANを含むTV放送のためのコヒーレント光学技術を説明されました。ハイト氏の主題は周波数分割多重TVまたは遠距離高精細度TV放送へのいわゆるヘテロダイン検波法の利用であり，その特徴は高い周波数選択度，迅速で効率的な同調性及び高い受信機感度であります。

　HHIでの研究は1981年に始まり，1986年までには，10チャンネルの実験システムが完成し，現在ではこの計画はRACEプロジェクトの1部になっており，Philips, Siemens , HHI, Plessey, LEP, 及びIMECのようなヨーロッ

パの大きな組織体がこれに従事しています。

　第2セッション（A）では，光学スイッチ及び光学的信号処理の技術の状況が討論されました。1番目の発表は，光学スイッチの最近の進歩という表題で日本電信電話の小林氏が行いました。遠隔通信におけるスイッチングの歴史に始まって，小林氏は音声，ビデオ，データなど各種の情報をすべて同時に取り扱うスイッチング技術，特に光学スイッチについての将来の対応を推測されました。同氏はまた，いわゆる周波数多重と時分割多重の組合せが将来有望であると推測されました。

　つぎに，Universität Münster のイエーガ教授がデジタル光学プロセッサーについて講演されました。教授は，この分野でのヨーロッパにおける計画とドイツ国内における計画の概要を説明されました。その計画というのは，「ヨーロッパ・ジョイント・オプティカル双安定性研究計画」の略称であるEJOB計画，及びデジタル光学プロセッサーについての他のBMFT，での試験研究であります。これらの計画において研究されている種々のデジタル処理技術が説明されました。

　「光情報処理」と題する3番目の発表は，光産業技術振興協会（OITDA）の石原氏が講演され，電子的方法と対比させて光学的方法の一般的な特徴を説明されました。

　石原氏はまず，最近の既存の情報処理システムに如何に光学的方法が重要な役割を演じているかを述べられました。それは例えば記憶装置としての光ディスクや光学カード，情報伝達の手段としての光通信，読込み設置としてのバーコード及び読み取り装置としての光ディスプレーであります。すなわち石原氏によれば，オプト・エレクトロニクスに残された唯一の未開拓分野は情報処理の分野なのです。

　石原氏はまた，過去10年間に日本ではオプト・エレクトロニクス産業が爆発的な拡大を遂げ，1987年度の総生産額は1兆 2,300億円に達し，これは全エレクトロニクス産業の生産額の約10％であるとのべられました。

　つぎに，HHIのハイト氏が光学スイッチ技術の現状を説明されました。過去及び近い未来の一般的動向の説明のあと，ハイト氏は種々のタイプの光学スイッチ，すなわち2次元，3次元及び周波数分割スイッチについて説明されました。ドイツ及びRACEプロジェクトに参加中のヨーロッパ諸国での研究活動を説明され，さ

らにこれらの研究プログラム中に開発されるべきスイッチング計画が，紹介されました。

このセッションでの最後の発表は，「光学的並列デジタルコンピュータ」と題して大阪大学の一岡教授が講演されました。教授は，大阪大学の自分の研究室で考案され開発されたOPALSという光学的並列論理アレイ・システムについて主に説明されました。

その動作の1例として，日本では「迷い路」と呼ばれている迷路の正しい回答を完全に光学的に算定する方法を説明され，聴衆に非常な興味を呼び起こしました。

第2セッション（B）の主題は，「社会的アクセプタンス及び情報セキュリティ」でした。これはやや社会科学指向の主題であります。1番目の発表は，「新情報化社会に於ける社会的アクセプタンス及びセキュリティ問題」という題で日本IBMの上園氏が講演され，情報セキュリティの問題についての考え方についての日本での一般的な状況を説明されました。そして，この主題について日本で行われた世論調査の結果を報告されました。その結論は，現在のところ日本人は一般に情報セキュリティの問題については，あまり意識していないということでした。

2番目の発表は西ドイツ郵電省のヴォルフェンシュテッター氏で表題は「ニューメディアにおける情報セキュリティ」でした。ヴォルフェンシュテッター氏はこの問題の理論的観点を説明されました。まず，セキュリティの問題を確実性の問題及び機密性の問題に分類し，西ドイツで現在進められている理論的研究について説明されました。

この第2セッション（B）の最後の発表は，mbp Software & Sysytems のシュレーダ氏で表題は「Electronic Signature as an Add On to the Teletex Service」でした。

電子署名（Electronic Signature）は，来たるべき情報化社会において極めて重要な技術になるでしょう。シュレーダ氏はドイツで開発中の興味あるこのシステムを説明されました。この分野に関してはドイツ人が日本人の数歩先を進んでいるように思われますし，日本の代表者は次回及びその次のフォーラムでドイツでの進歩についてもっと話しを聴きたいと感じました。

「ICカード，光カード及びCD－I，CD－ROMを含む新情報メディア」という表題の第4セッションは，「データ放送」という表題の日本放送協会の柳町氏の講演で始まりました。データ放送というのは，多分あまりよく知られていない概念であります。歴史的には，放送の対象は音声と音響から進歩して白黒のテレビジョン画像となり，つぎに完全なカラー画像になりました。将来出現すると思われるデータ放送は，符号化された情報が加入者のパーソナル・コンピュータに送られるという，放送の新しい様相であります。情報の内容はファクシミリ画像，コンピュータ音楽，パソコンのプログラム，データなど多岐にわたっています。

　2人目の講演者の西ドイツ郵電省のハンメル氏で，西ドイツ郵電省によるデータ放送の導入という題で話をされました。最初のデータ放送は実際にはいわゆるページングサービスといわれ，ユーロシグナルという名称で，1974年にフランス及びスイスと共にドイツで開始されました。これまでに 140,000人の加入者を獲得し，西ドイツ郵電省ではCTルーフと呼ばれるUHFラジオ通信用電波を使った新しいページング業務のための開発計画が，今年末に始まろうとしています。また，次の目標は現在，西ドイツで開発中の衛星を使ったデータ配送サービスであります。

　つぎの3番目の発表は，「光カードの最近の進歩」という題の，オリンパス光学工業のウイリアムズ氏の講演でした。光カードは，標準的に1枚あたり2メガバイトの記憶容量を持ち，製造コストが安く大量生産できるのが特徴です。読み出し専用の光カードは，例えば小容量の電子出版に使用できます。読み出し／書き込み型のものには，医療カルテ，身分証明書，銀行カード及び保険などにわたるもっと広範囲な用途があります。

　4番目の発表は西ドイツ郵電省のヴォルフェンシュテッター氏で，表題は「チップカード　― 機能と用途 ― 」でした。チップカードというのはとりもなおさず日本でICカードと呼ばれているものです。ICカードすなわちチップカードの歴史は1983年に遡ります。その後5年間，僅か5年の間に実に急速な進歩があり，ICカードは今やキャッシュレスの買い物，コインレスの電話通話，医療情報の記憶などの種々の用途に，また身分証明書としても使用されるようになりつつあります。

５番目の発表は，「日本におけるＣＤ−ＲＯＭの現状」という表題で，新学社の堀内氏が講演されました。ＣＤ−ＲＯＭとは，コンパクトディスク読み出し専用メモリーの略です。堀内氏によれば，ただ１枚のコンパクトディスクが驚くべき容量を持ち，莫大な量の情報を記録できます。例えば，書類 250,000頁分，または書籍 2,000 冊分，またはフロッピーディスク 500枚ないし，1,000 枚分，または磁気テープ10本分に当たります。その上，例えば１枚３ドルとコストが非常に安く，ＣＤ−ＲＯＭは電子出版において強力な武器になりつつあります。

　この最後のセッションの最後の発表者は，西ドイツ郵電省のシュタイナー氏でした。発表の表題は，「ビジネスの分野におけるビデオ通信」でありました。ビジネスの分野における高品質のビデオ通信は，広帯域通信の導入における重要な戦略分野であります。最初の主な用途であるビデオ会議は，既に主な先進国で導入されています。

　結論として，私は２つの点を強調したいと思います。第一に，両国の技術と社会環境に関する類似点や相違点が今回の討論で非常によく理解されました。第２に，私が個人的に感じましたことは，私達日本人は比較的，機器や設置の製造に強く，それに対してドイツ人が社会と人間生活の利益と向上のために技術進歩の成果を実生活に利用することに極めて巧みであるということであります。

　このセッションは非常に実り多いものであったと信じております。この機会にドイツ側のニューメディア共同議長であるＨＨＩのバーク氏及びコアメンバーの皆様，そしてご出席の皆様のご協力に深く感謝いたしますとともに，皆様方のご好意に深く感謝申し上げます。ありがとうございました。

3.2　コンピュータ分科会
〔コンピュータ分科会日本側主査　相磯秀夫〕

　コンピュータ分科会では３つのセッションを持ち，それぞれのセッションにおきまして原則として２つの話題をそれぞれの国から出し，討論には然るべき時間を充てられるようにしました。

　第１セッションは「オペレーティング・シムテムとリアルタイム・システム」と

いう表題でＴＲＯＮ計画の概観から始まりました。ＴＲＯＮ計画は，東京大学の坂村健助教授の指導による民間の意欲的な計画であり，日本ＩＢＭのような外資系企業を含む 118社で構成される非営利組織によって実施されています。

この計画の目的は，家庭，事務所及び産業機関を含む総合的なコンピュータ文化を創造することであり，誰でも簡単に使えて，人間中心に設計されている点に特徴があります。

講演者である日立製作所の伊藤氏は，この計画の背景，動機並びに潜在的な特徴を紹介され，また既に市場に出ている32ビットＴＲＯＮマイクロプロセッサーの開発を含むサブプロジェクトも紹介されました。

続いて，日本電信電話の石野氏がＣ－ＴＲＯＮの研究開発に関する講演がありました。Ｃ－ＴＲＯＮ計画は，ＴＲＯＮ計画の最も重要なサブプロジェクトの１つであります。石野氏は，まずコンピュータと通信の影響について述べ，その効果的な実施のために幾つかの層からなる階層構造について論じ，最後にＣ－ＴＲＯＮの特徴を紹介しました。

ドイツ側からは，ＧＭＤのグース教授が現在ＧＭＤで開発中のBirlixオペレーティング・システムについて講演されました。グース教授はまずＵＮＩＸの中枢機能の不足を指摘され，この計画の目的を紹介されました。この計画は，現行のＵＮＩＸオペレーティング・システム中枢の機能不足を補うことを目的としています。設計の原理は，オブジェクト指向及び拡張可能という概念に基づいており，そのインタフェースはネットワーク指向機能の導入と機密保護，及びフェイルセーフ機構の実装に特に重点を置いており，現在のバークレイＵＮＩＸに対応しています。それはポストＵＮＩＸのオペレーティング・システムと思われます。

第１セッションの最後の講演は，Siemens のゲバルト氏のＸ／Open：OpenＵＮＩＸ環境の紹介でした。ゲバルト氏はＵＮＩＸ　ＯＳ分野における事実上の標準規格の定義とその意味について説明しました。また非営利的な研究開発コンソーシアムで行われている国際的なＸ／Openプロジェクトを紹介されました。Ｘ／Openの目的は，現存の標準規格または事実上の標準規格を共通の利用環境に適応させ採用することであって，新しい規格をつくることではありません。Ｘ／Openは，ＰＯＳＩＸ，

プログラム言語，データ管理，ユーザー・インタフェースなどのような現存オペレーティング・システムのインタフェースの標準化に焦点を当てています。

　第2セッションでは，高度情報技術の応用についての最近のトピックスについて討議されました。このセッションの最初の講演は日本の特許庁の石井氏の行ったオープンシステムの接続（OSI）概念に基づく電子特許出願システムの説明でした。この計画の目標は，日本での書類提出によらない電子式特許出願制度の受け入れにあります。石井氏は，そのような大規模なシステムの開発の必要性を説明され，システムの構成を紹介されました。このシステムは，OSIプロトコルの規格に基づいて設計され全国的な大規模ネットワークと多数の高性能ワークステーションから構成されています。これは，1990年の春先からの使用が予定されています。

　三井銀総合研究所の岩丸氏は，世界中で最も進んでいると認められている，日本の国際オンライン銀行業務システムについて講演されました。岩丸氏は日本の銀行業務システムの過去，現在及び未来を紹介されました。まず銀行業務の分類に始まって将来実施されるべき銀行業務システムの必要条件を指摘されました。また，3世代にわたるコンピュータ・ネットワーク及び情報処理システムによって支えられた日本の銀行業務のサポートについて詳しく説明されました。

　現在の第3世代三井銀行業務システムは，世界中に接続されたコンピュータ・システムですが，地震による緊急災害にそなえて，同じバックアップ・コンピュータ・システムを他に準備しています。

　ドイツ側からは，University of Saarbrucken のヴァルスター教授が知識ベース応用システムのためのインテリジェント・インタフェースについて興味ある講演をされました。ヴァルスター教授は，図形，ジェスチャー，自然言語，メニュー，スケッチング及びビデオが扱える高度な機能を持つエキスパートシステムに対するマルチモーダル・インタフェースの説明をされました。教授は，日本で研究の努力がほとんどされていないヒューマンインタフェース研究の重要な役割を強調されました。講演は，ドイツにおける他のインテリジェント・インタフェース計画の概要についても話されました。

　Siemens のホーヴァイン氏は，工業オートメーションにおける知識ベース技術に

ついて講演されました。工業オートメーションの複雑化にともない，コンピュータ支援設計（ＣＡＤ）及びコンピュータ支援製造（ＣＡＭ）の開発に対する要求が急速に高まってきております。ホーヴァイン氏は，工業オートメーション，特に圧延機のオートメーションにおける有用な知識ベースシステムの幾つかの例を紹介されました。また，知識取得，ドキュメント処理及びその提供に使われるエキスパートシステムの利用について説明され，効率向上の評価を通して開発されたシステムの有用性を実証されました。

　第3セッションでは，大阪学院大学の大村教授が映画及びアニメーションの製作に使用されるＬＩＮＫＳ－２と称する専用マシンの概要を説明されました。アニメーションや映画の製作には普通膨大な計算時間がかかり，しかも芸術家にも複雑な仕事の負担を与えるものですが，そのような厳しい問題を軽減するためにこの計画は始められました。提案されたマシンのアーキテクチャは，むしろ簡単なものですが，自動アニメーション作業のために特殊化されたものであります。この専用マシンは近い将来，約1000台の処理装置から成る強力な大規模マルテプロセッサ・システムになるはずです。大村教授はまた，芸術家のようなコンピュータの専門家でないユーザが専門の知識なしにシステムを使えるような，簡単で使いやすいユーザ言語を提供するとの必要性を説明されました。

　電子技術総合研究所の樋口氏は，セマンティック・ネットワーク・マシンＩＸＭの計画について概要を説明されました。セマンティック・ネットワークは，人口知能問題にしばしば見られる知識の階層構造を理解するのに便利です。しかし，一般にセマンティック・ネットワークの処理には時間がかかり，普通のコンピュータではセマンティック・ネットワークに含まれる潜在的な並列性を効率的に利用することができません。樋口氏は，この問題を解決するため，セマンティック・ネットワークを効率的に処理するために多数の連想メモリを持つ大規模な並列処理アーキテクチャを提案しました。同氏は設計理念，機能の特徴及びアーキテクチャについて説明し，シミュレーションによって期待される性能を提示されました。

　ドイツ側からは，ＳＵＰＲＥＮＵＭのゾルヘンバッハ氏がドイツの科学計算用スーパーコンピュータを紹介されました。スーパーコンピュータは，学問及び産業の

両分野で必須の道具であることが認められており，そのため種々のプロジェクトが各国で活発に行われています。

　ドイツのスーパーコンピュータは，ＳＵＰＲＥＮＵＭ研究所という名の共同体で開発され，そのスーパーコンピュータはすでに市販されています。同氏はまず，応用プログラマーの観点からスーパーコンピュータについて重要な分類カテゴリーについて説明され，ＳＵＰＲＥＮＵＭのアーキテクチャ，ハードウェア，ソフトウェア，及びＳＵＰＲＥＮＵＭのスーパーコンピュータの将来の構想を紹介されました。

　第３セッションの２番目の講演者としてＧＭＤのジロア教授が，順次プロローグ言語の並列処理のためのアーキテクチャについて説明されました。このシステムは並列演算のプロローグ・エンジンが付加された通常のＵＮＩＸワークステーションから成っています。エンジンは最適化された順次プロローグ・プログラムを実行するように設計されたパイプライン方式のユニフィケーションプロセッサから成り立っています。提案されたアーキテクチャは簡単なように思われますが，実際の観察に基づいて設計されたものです。これは現存の単一プロセッサーのプロローグマシンに比べて速度において決定的な利点をもっています。

　第３セッションの最後に，University of Mainz のフォン・ジーレン教授がニューラルネットにおける計算と題する講演をされました。ニューラルネットの概念は，例えば多次元最適化問題，イメージ処理やパターン認識の研究に有効であることがよく知られています。また，ニューラルネットワークが大規模並列計算処理と密接な関係にあることを指摘しました。それは耐故障性の向上とゆるやかな性能低下を伴なう連続稼働の可能性を与えます。フォン・ジーレン教授は，計算ステップ，信号の冗長性の利用及び信頼度などの点について工学的システムと生物学的な神経系との関係を説明されました。そして，生物学的な情報処理の実例を示し，生物学的システムに見られる類の並列処理が，例えば，ビジョン処理に使用される工学システムにも活用できることを説明されました。

　結論としまして，今回のフォーラムはお互いに有用な情報の交換が，でき，大変有益なものでありました。講演者並びにセッションの運営に関与されました方々に厚くお礼申し上げます。有難うございました。

3.3 半導体分科会

〔半導体分科会日本側主査 菅野卓雄〕

　半導体分科会で行われました各発表を要約したいと思います。ドイツ側の半導体グループを統括されているルプレヒト教授が今年はご病気のため来日されなかったのは残念でございます。しかし，私たちはこの2日間本当に有益な研究会を持つことができました。

　今年，私たちは3つの主題に議論の焦点を当てたいと考えました。その第1は特に遠距離通信用への半導体技術の応用であります。それで，第1セッションの表題は「ミリ波IC」及び「光データリンク」でした。また，私たちはⅢ−Ⅴ族半導体技術の将来の見通しについてアイデアを得ようと思いましたので，第2セッションの議題は将来の情報システムにおけるⅢ−Ⅴ族化合物半導体デバイスの役割ということになりました。もちろんシリコンは高速度デジタル用途でもⅢ−Ⅴ族化合物半導体と競合しますので，第3セッションはサブピコ秒シリコン・オプトエレクトロニック・スイッチを含む高速度シリコンデバイス及び回路でした。

　第1セッションの「ミリ波IC」及び「光データリンク」では，ミリ波ICまたは30GHzVANについて2つの発表がありました。

　最初に日本電信電話の加藤氏，つぎにAEGのメンツェル氏が発表され，かなりよく似た技術開発が両国で行われていることがわかりました。日本では，加藤氏が衛星応答機用のモノリシック・ガリウム砒素ICを説明されました。加藤氏は，主要モノリシック・マイクロ波ICのためのこれらの5割のガリウム砒素ICが0.3ないし0.5ミクロンゲートのガリウム砒素MESFET及びショットキー・バリアダイオードを使用していることを報告されました。

　メンツェ氏の発表でも，ガリウム砒素MESFET及びショットキー・バリアダイオードからなる35GHz受信機チップが報告されました。メンツェル氏は，周波数範囲を35GHzから60さらに94GHzにまで拡げる努力について報告されました。この努力にはHEMT増幅器の使用も含まれています。

　3番目の発表もミリ波ICでしたが，遠距離通信用だけでなく種々の用途につい

てでした。この発表では，工学試験衛星6号のためのミリ波送信システムが報告され，このシステムには38GHzでの出力が0.5ワットの固体高出力増幅器と43GHzでの雑音電波が4.8dBの低ノイズの増幅器が含まれています。

第2の用途は，核融合研究用の日本の原子炉であるJT60中でのプラズマの電子温度を測定するためのミリ波送信システムを使ったプラズマ診断であります。

またもう1つの用途は大気中の伝搬の測定であります。このシステムでは2つの周波数が使用されました。すなわち2つの周波数の間の相互の位相シフトを測定するために80及び 240GHzが使用されました。2つの周波数はもちろん位相の差を測るために干渉性であります。この興味あるデバイスは，アルミニウム・ガリウム砒素のヘテロMISゲートFETであり，このデバイスの性能の特徴は38GHzで8.1dBという高い信号出力利得がえられたことであります。

第1セッションの最後の発表は，SELのハイデマン氏でした。ハイデマン氏は，光伝送技術の進歩並びに，毎秒5ないし10ギガビット伝送及び未来システムの可能性，すなわち高速度信号処理技術の能力の可能性とシステムの限界と概要について極めて広範の議論を行われました。もっとも顕著な成功はドイツで達成されました。それは，分散シフトシングルモード光ファイバーを使った 111キロメートル用の5ギガビット／秒の光通信であり，1.55ミクロンの分散フィードバックレーザが使用されています。この成功は同氏自身によって達成されました。

つぎにガリウム砒素技術の将来について論じることになりました。これは，三菱電機の柴山氏が講演されました。ガリウム砒素LSIの利用の動向および光コンピュータの話から始められ，そのあと，ガリウム砒素と光デバイスの技術動向が説明されました。現在ガリウム砒素ICを使用している実用的なデバイスは，ご存じのようにMESFETですが，3年以内にHEMTや自己整合型のFETが多分実用化され1995年にはヘテロバイポーラ・トランジスタがガリウム砒素ICに使用される実用的なデバイスになるだろうと述べられました。光デバイスの分野では，二重ヘテロ接合レーザが現在実用されていますが，ここ2，3年の内に量子井戸レーザが使われるようになるでしょうし，1993年には量子井戸レーザや量子ワイヤー，量子ボックスが使用されるでしょう。この討議はガリウム砒素デバイスのそのような

未来の展望について行われました。

　何人かの人は柴山氏が光デバイスの将来についてかなり楽観的であると感じたでしょう。しかし，今朝私はTVと新聞で三菱電機が機能，光接続を持つメモリチップをガリウム砒素で実現したことを発表したことを知りまして，同氏がガリウム砒素IC技術への光技術の応用に自信をもっておられることがわかりました。同氏は過去に予測された市場はあまりにも楽観的すぎるとも言われました。今年の実際の市場規模は予想のちょうど半分であります。

　2番目の発表は，Siemens のプラッデル氏でした。同氏は，将来の情報システムにおけるガリウム砒素の役割について述べられました。プラッデル氏は，半絶縁性ガリウム砒素の品質を向上させる努力を報告され，ガリウム砒素へのベリリウムのドーピングの有用性を強調されました。鉄ドーピングのデバイスでは，個別デバイス，小信号マイクロ波及びデジタルIC及びエピタキシャルデバイス，HEMTのパワーデバイスなどが説明されました。

　重要な成功の1つは，0.5ミクロンのデバイスの製造にI－ラインステッパーを使うことでした。つぎに，富士通研究所の太宰氏がHEMT及び関連の新しいデバイス技術を説明されました。同氏は，現状と将来の動向及び将来の高速度システムに対するこれらのデバイスのインパクトの可能性を説明され，これらのデバイス技術の分野における富士通研究所の大きな成功について説明がありました。例えば低ノイズHEMTは現在20GHzで1.8dBの雑音指数であり，HEMT，LSIの例として16Kbit SRAMがHEMTで構成されています。このSRAMのアクセス時間は77°Kで3.4ナノセカンドであると報告されました。

　優れた成果の1つは，ヘテロバイポーラトランジスタによる高速度スイッチングです。太宰氏は，2.6ピコ秒の遅延をゲートあたり60ミリワットの電力消費で達成したと報告されました。私の知る限りでは，これは接合デバイスで得られた最高の速度であり，ほぼジョセフソン接合技術に匹敵するものである。

　共鳴エミッタRをもつホット・エレクトロントランジスタはRHETと呼ばれ，機能デバイスの一種であり単一のデバイスで排他的論理和回路を造ることができ1ピコ秒のスイッチングの達成が期待されています。

4番目の発表は，ＭＰＩのラムスドルフ氏でピコ秒のシリコンスイッチの説明でした。ラムスドルフ氏は，ＳＯＩ構造を使用したシリコン・スイッチで88フェムト秒のレーザーパルスから１ピコ秒の電子パルスが発生することについて報告されました。このＳＯＩは，キャリアの寿命が０．５ピコ秒にまで短縮されるように，サファイアの上に0.5ミクロンのシリコン膜を堆積させたものであります。

　最後のセッションでは，シリコン・デバイスの将来の見通しについて討論しました。１番目の発表は，高速度シリコン・バイポーラトランジスタの分野でよく知られた研究者である日本電信電話の酒井氏です。同氏のお話は超高速度ＬＳＩのためのバイポーラ技術に集中されました。

　昨日，酒井氏は選択的イオン打ち込みコレクターいわゆるＳＩＣを持つスーパー・セルフライン・トランジスタの新しい構造を報告されました。ＳＩＣ製造を使う事によってf_Tは従来のスーパー・セルフライン・トランジスタのほぼ半分に低減できます。またＳＩＣ構造を使うことによって高電流密度におけるベースのプッシュ・アウトが避けられました。それで，ＳＩＣ構造によってスーパー・セルフライン・トランジスタ（ＳＳＴ）は，21ないし26ＧＨｚという高い遮断周波数とゲートあたり25ピコ秒のスイッチングが達成できることが示されました。

　つぎに，Siemens のクローゼ氏も高速度シリコン・デバイス及び回路についての報告をされ，バイポーラ技術について非常に広範囲にわたる議論をされました。同氏の結論は，バイポーラトランジスタが高速度回路の中程度の複雑さに大変適しており，バイポーラ技術の動向は25ＧＨｚより高い遮断周波数を得るため，Ｂｉ－ＣＭＯＳ技術が複雑な回路に最適であるということであります。また氏はＢｉ－ＣＭＯＳ技術の現況についても説明されました。256Kbit ＳＲＡＭが日立製作所とＴＩで製作，開発され，また１メガＤＲＡＭが日立製作所で開発されました。

　Ｂｉ－ＣＭＯＳの動向とともに，ＥＣＲとＣＭＯＳの組合せ，そして他のマイクロセルの応用が有効となると期待されています。

　次に，日立製作所の武田氏がＶＬＳＩを超すＵＬＳＩ，ＵＬＳＩ－ＭＯＳデバイスの現状と将来の見通しについて講演され，64メガビットＤＲＡＭのための技術革新が0.3ミクロンの技術を使って開始され，ＩＢＭは最近，スタティック論理回路

で0.1ミクロンゲートのMOSFETを用い10ピコ秒より短いスイッチング遅延の達成を発表したと説明されました。

　現在の時点ではDRAM用MOSFETには0.3ミクロン，論理用には0.1ミクロンが実用的な目標でしょう。博士はまた，0.1ミクロン未満の厚さの極薄のシリコン膜で造られているSOIデバイスが将来のMOSデバイスに非常に有用であることを強調されました。SOI構造を使うと短チャネル効果の抑制が期待されるからであります。武田氏はまた，シリコン・デバイスでの量子効果の可能性を述べられました。そのような量子効果はチャネルの長さが0.1ミクロン未満の小チャネルデバイスで観察されます。

　量子効果の例は，ドーパントの不純物の統計的な変動であり，このためMOSFETのしきい電圧が変動し，チャネル内で電子の速度のオーバーシュートがあり，またチャネル内でのコンダクタンスの異常な変動が起こります。

　最後の発表は，AEGのカスパー氏のよって行われました。氏は，シリコンの低温分子ビームエピタキシ法の広範な議論ともちろん同氏自身の研究を説明されました。現在 (100)シリコン表面で 150ないし 300℃という低い最低エピタキシャル温度が報告されており，もっとも顕著で目ざましい効果は，シリコンゲルマニウムの格子構造の層の中のホール移動度の増加であり，また超薄膜のシリコンゲルマニウムのスーパーラテイス内の直接遷移の著しい増加であります。

　この直接遷移の著しい増加は，オプトエレクトロニクスの分野へのシリコンデバイスの利用の新しい可能性を開くものであります。

　以上が半導体分科で行われた発表の要約であります。私は各発表者の方々に対して当然申し上げるべき賞賛の言葉に欠けるところがあったかもしれません。お許し下さい。ご協力有難うございました。

4.　閉会挨拶

4. 閉 会 挨 拶

4.1 柳井久義　日本側議長　芝浦工業大学学長

　それでは閉会の言葉を述べさせていただきたいと思います。私に続きましてエン
グル議長もご挨拶をされますので，重複をさけるため私はおもに日本人の方々に日
本語でご挨拶させていただきたいと思います。

　おはようございます。日本の皆様たいへんありがとうございました。お陰様で，
ただ今の各分科会の報告のありましたとおり，たいへん有効なフォーラムが持てま
したことをうれしく思っておる次第でございます。今後ともこのフォーラムを発展
させて，日独友好のためにさらにご協力いただきたいと思います。

　フォーラムの各分科会は今報告があったとおりでございますが，このフォーラム
の間におきまして，次回以降のフォーラムの在り方という問題を，各分科会チェア
マン並びにコアメンバーの方々及び研究技術省と通商産業省の方々とご相談してま
いりました。その結果といたしまして，従来どおりこのような方式で，少しずつ改
良を加えながら発展させて行こうと言うことについては意見が一致しております。
すなわち，その場合，相互に有益かつ適切なテーマを選定して行こうではないかと
いうこと，また必要によってはセミオープン方式でフォーラムを開催して行くのも
良いのではないかということ，あるいは，各分科会ごとに運営方式がある程度違っ
ても良いのではないかというようなことなど，このような改善をしながらさらにフ
ォーラムを発展させて行きたいというふうになっております。

　一方におきまして，両国の研究協力あるいは共同研究を導入していくようなこと
も，フォーラムの成果として挙げていきたいということが話あわれました。これは，
このフォーラムの発足時から望まれていたことでございます。お互いの情報交換，
あるいは，人的な友好関係の強化という点ではかなり進んでまいりましたので，ぼ
つぼつ両国の研究協力とか共同研究のようなものに発展させることも考えていった
らどうだろうかということでございます。そこで取りあえず次のような形で始めて
みたらどうかということであります。取り上げる分野は，当然インフォメーショ
ン・テクノロジーの範囲に限定する。それから日独を主体とした２国間協力を主体

にする。しかし必ずしもそれにこだわるものでもない。さらに，これは急には行き
ませんが，新しく国あるいは産業界からの援助を求める。しかし既存の制度はでき
るだけ積極的に利用して行くようにする。ただそういうような形の援助ということ
にはあまりとらわれないで，お互いに研究協力，あるいは共同研究を進めてみる
ことを考えてみようではないかということであります。そのためにまず，両国にとっ
て協力が望ましいと考えられるような基礎研究分野につきまして，そういう問題が
あるかどうかというのを抽出してみる。そして，そういう分野，問題で両国のコア
メンバーの方々が，自分の国の中で関心が高くて積極的に研究を進めておられるよ
うな機関とか研究者とかを調査してみる。その調査結果をお互いに交換しあい，よ
く検討を加え，また，そういう機関あるいは研究者の方の希望もできるだけお聞き
した上で，協力できそうな具体的研究を見いだして，研究協力をその当事者，機関
なりにお勧めして行くというようなことを考えてみたらどうだろうかということで
ございます。そういうような研究題目がでてきました場合には，それをプロジェク
ト研究のような形で推進するため，その当事者同士が研究計画，成果や進行状況な
りを時々情報交換しながら研究を進めてゆくこととする。この場合に，研究者が相
互に短期間，すなわち１ないし３カ月くらいの短期間で，相手方の研究の場に出張
して協力の実をあげるというのは望ましいのではないか。また，コアメンバーの方
々は，そういう共同研究あるいは研究協力をしておられる方々に対して，適当なる
助言を与えるとか，適宜支援をするというような立場をとるべきではないかという
ふうに考えられます。さらにそういうものが進行してまいりましたら，それをフォ
ーラムの場でご報告していただくというようなことも考えてみたらどうだろうかと
いうことになってまいりました。そこで，それらのための準備もございますし，１
年毎というのはちょっと間が短すぎるという点もございましたので，次回のフォー
ラムは間を１年半おきまして，1990年の春にしようかということになりました。場
所につきましては，次回はドイツでございますが，後ほどドイツの方でいろいろお
考えいただくということでございます。以上，将来の問題につきまして，現在その
ような方向で動いておりますということをご報告申し上げ，皆様のご協力を得たい
と思いますのでよろしくお願いします。

最後に，ドイツ側の参加者の皆様方に，今回フォーラムに友好的かつ積極的にご参加いただき，活発で内容豊かなディスカッションをしていただきましたことを心よりお礼申し上げます。そして，われわれの活動と友情が，今後のフォーラムに向けても，より深められることを願うものでございます。どうもありがとうございました。

4.2　ワルター・L・エングル　ドイツ側議長　アーヘン工科大学教授

　日独情報技術フォーラムもその5年間にわたる第1段階を経過してきました。その実施方法の形態にもある種の連続性が生み出されましたが，その形態は今後とも保たれるべきであり，また他面ではさらに拡大されるべきものでもあります。これまでの形態の中では，自分自身が講演を行うためにフォーラムに参加するわけではない参加者の輪を広げようとする試みを，既に先年，シュツットガルトで行いました。

　実施した場所からして当然となりますが，そのシュツットガルトで，諸機関の若い研究者が大勢，講演やディスカッションに参加していただきましたのは，大変素晴らしいことでありました。これは評価を得たものと思いますし，またこれを恒常的な形態とするべきであると思います。

　しかし，さらに重要なのは，両国の共同の研究プロジェクトの実施を試みることによって共同作業をさらに拡大しよう，また，この両面からの共同作業を進渉させるにあたっては以下に述べるような形であるべきだと決議したことであります。

　まず，研究テーマの選定は，国家や企業からの要請から影響を受けること無くなされるべきであるということ。もちろん，そのような国家や企業からの援助は望ましいものではありますが，それはボトムアップ・アプローチによって，既存のプログラムに左右されることなくテーマの提供が行われるべきであります。そして，そのようなテーマを推奨プログラムとしてとりまとめる努力がなされるべきであります。また，われわれは，その作業を行うに当りBMFT（研究技術省）による支援も希望します。その際，コアメンバーは，これまで以上に義務が課されることになります。

つまり，分野の選択では指揮監修の責任があり，またその都度日本のコアメンバーと協力して，両面からの提案の比較を行い，研究所または個人によって共同で行われるプロジェクトのために作成されるリストから共通点を見つけ出す必要があります。

　その場合に，比較的短期に，といいましても1カ月から3カ月ぐらいの期間になるでしょうが，交互に訪問滞在して，進行中のプロジェクトについてアクティブな情報交換を行う，ということが考えられています。そしてコアメンバーは，プロジェクトの実施にあたって全面的な支援の態勢でいる，つまり名付け親，後見人の役割を引き受けていただく事になります。

　最後にこのプロジェクト研究の経過や成果については，フォーラムの場で報告が行われます。このような共同作業から，私達は活動のさらなる強化を，そして何よりも，若くして新鮮な血によってフォーラムがさらに活性化されることを望みます。

付録１　基調講演アブストラクト

「Neurocomputing」
　　　松本元　電子技術総合研究所

「Integrated Optoelectronics for Communications 」
　　　クラウス・ワイリッヒ　Siemens

付録 1. 基調講演アブストラクト

NEUROCOMPUTING ————

NEURONS AS MICROPROCESSORS WITH

A KIND OF MEMORY FUNCTIONS

Gen Matsumoto

Electrotechnical Laboratory
Tsukuba City, Ibaraki 305
Japan

INTRODUCTION

Studies on neurocomputing (Amari, 1982; Rumelhart *et al.*, 1986a) should be directed in two ways which in turn influence each other (Matsumoto, 1988): In one direction concrete neural-network solutions for specific important problems should be applied to substantiate its practical significance and, at the same time, the theoretical potentialities and limitations for computation should be explored on such network models. The alternative way is to seek a more profound understanding of the algorithms used by the CNS (central nervous system) to process information and to learn more about the molecular and cellular mechanisms underlying specific computations and memory processes in neurons and neural networks.

We will first give a brief review of current research on neurocomputing. The potentialities and limitations of neurocomputing will be discussed. We stress that these limitations primarily originate from the oversimplified model of a neuron (an artificial neuron model). We note that electrical events occurring in a natural neuron are part of the manifestations associated with neural activities and are regulated by the chemical and conformational processes inside the neuron. Neurons could correspond to LSI (large-scale integrated) microprocessors with a kind of memory function in the electronic digital-computing system. A concrete example of the neural information processing at the synaptic sites will be given for the primarily-cultured neurons of both rat hippocampus CA1 pyramidal cells and rabbit superior cervical ganglion cells. The information processing performed at the synaptic sites will be discussed from the standpoint of computational science. Finally we will discuss how we should proceed in the neuroscientific study of neurons and neural networks for information science.

NEUROCOMPUTING –COMPUTATIONS PERFORMED ON ARTIFICIAL NEURON NETWORKS-

The Artificial Neuron Model

The current models of artificial neuron networks are neurally inspired mathematical models that use a large number of simple, homogeneous but highly-interconnected processing elements, "artificial neurons". An artificial neuron collects inputs, using its internal summer after each of them is multiplied by its proper weight, and produces an output only if the

sum of the inputs exceeds an internal threshold value. We shall call the computing performed on these neural networks "neurocomputing". The operation of the current models of the neural network is basically nearest-neighbour search. The efforts of research on neurocomputing have been concentrated on searching the efficiencies of these neural networks in performing this operation (Amari, 1982; Kohonen, 1984; Rumelhart *et al.*, 1986a) and on applying concrete neural network solutions for specific problems to substantiate the practical significance (Hopfield and Tank, 1985; Sejnowski and Rosenberg, 1986).

The Error Back-Propagation Model

Recently Hecht-Nielsen (1986a) has shown that a three or more-layer neural network system can generally represent the connection strength that will give the appropriate output for all inputs. In other words any continuous mapping from input to output can be done in a three or more-layer system. The problem now is how to implement a learning procedure for a multi (three or more)-layer system. If the input units are directly connected to the output units, it is relatively easy to find learning rules that iteratively adjust the strengths of the connections so as to pro-gressively reduce the difference between the actual and desired output vectors (Minisky and Papert, 1969). Learning becomes more interesting and more difficult when we introduce a multi-layer network with hidden units whose actual or desired states are not specified by the task. The reason the learning becomes more difficult arises from the requirement that the learning procedure must decide under what circumstances the hidden units should be active in order to help achieve the desired input-output behavior. The reason the learning becomes more interesting is because the learning procedure itself is a means to construct a new representation. Rumelhart, Hinton and Williams (1986b) have constructed a novel algorithm which gives an effective learning procedure for the neural network with hidden units. In the three-layer system, the weights are adjusted for the output layer according to an error function that calculates a weight adjustment based on the difference between the actual and desired outputs. In other words, each error value for each actual output unit is propagated backward to the hidden layer and used to adjust the values of the weights to the hidden units. The procedure repeatedly adjusts the weights of the connections in the network so as to minimize the error function (a measure of the difference between the actual and desired output states). As a result of the weight adjustments, internal hidden units come to represent important features of the task domain, and the regularities in the task are captured by the interactions of these units. Practical usefulness of the learning procedure of the back-propagation model was demonstrated by Sejnowski and Rosenberg (1986). They constructed a neural network applica-tion of NETalk that did text-to-speech conversion of English. The network consists of three layers of artificial neurons; the input, the middle (or hidden) and the output layers contain 203, 80 and 26 neurons, respectively. After the learning, the network captured the text-to-speech rule and successfully operated for the new text that was different from the one used for the learning. The network has achieved 95 % accuracy. The network performance was limited to 82 % accuracy without hidden units but was enhanced to 98 % by increasing the number of hidden units to 120. This example illustrates the usefulness of the error back-propagation learning algorithm and the value of the hidden units.

However, one of the disadvantages inherent in the error back-propagation learning procedure is that it cannot generally escape from local minimum states characterized by a set of quasi-stable states in the neural network system. The other disadvantage is that the time necessary for the learning becomes tremendously longer for large size problems. According to Hinton (1987), the time of the N-interconnected network necessary for the learning process should be on the order of N^3 when the

operation is executed on current serial digital computers. The time is reduced by the order of N when each weight of connection is separately calculated with a parallel computer. Therefore, one solution to overcome the disadvantage is to build a computer which is architecturally suited to handle the neural network system. Because the neural network is massively parallel in nature, a compuer built with several ten or hundred thousands of processors, where each processor takes the place of an artificial neuron, would improve the disadvantage. Many attempts are being made at building parallel computers for neural network systems (Hecht-Nielsen, 1986b). The other solution to overcome the difficulty of necessitating tremendously longer time in the learning for large size problems is to improve the learning algorithm of the error back-propagation model or to create a new learning algorithm to reduce the time. Most research efforts in neurocomputing are currently being devoted to the development of improved or new algorithms.

INFORMATION PROCESSINGS IN A NEURON

A neuron is a basic element for transmitting, processing and storing information in neural systems and the brain. The CNS is not composed of neurons with the homologous characteristics as has been assumed in the aritificial neuron. Rather, the variety is one of the most prominent characteristics of the neurons. Over 50 kinds of functionally different neurons are reported in the cerebrum. This variety may be tremendously increased when the functions possessed in neurons are analyzed in more detail. The versatility is another peculiar characteristic of neurons. Indeed, dynamic molecular transformations within a neuron take place by environmental stimuli and conditions, as shown below. Both the variety and versatility are inherently associated with the neuron. As a result, a neuron could be regarded as a kind of microprocessor with multiple information-processing (synaptic) sites and with a kind of memory function.

Here we will exemplify how the information is processed and stored in a neuron for both rat hippocampus pyramidal CA1 cells and rabbit superior cervical ganglion cells.

Rat Hippocampus Pyramidal CA1 Neurons

Pyramidal CA1 Neurons of the rat hippocampus all contain glutamate receptive sites which respond excitatorily. Besides the glutamate receptors, some of the neurons contain muscarinic acetylcholine (ACh) receptors. In muscarinic responses, ACh usually works excitatorily (Swanson *et al.*, 1982) but in some cases inhibitorily (Brown and Adams, 1980; Egan and North, 1986). These two opposite effects of ACh result from interactions of ACh with two different subtypes of ACh receptors (Egan and North, 1986); M_1 and M_2 subtypes (Fig.1). The subtype is characterized by its dissociation equilibrium with pirenzepine. The dissociation constants of the subtypes, M_1 and M_2, are ~10 and ~600 nM, respectively, for slices of rat pons containing the nucleus parabrachialis (Egan and North, 1986). ACh bound to the M_2 receptor causes membrane hyperpolarization as a consequence to an increase in the membrane conductance to potassium ions. The Ca^{2+}-dependent potassium channel couples to the M_2 receptor. On the other hand, ACh bound to the M_1 receptor brings about membrane depolarization as a result of a decrease in the potassium conductance. The potassium M channel is coupled to the M_1 receptor. Thus, presence of multiple receptive sites specific for a neurotransmitter augments the variety of the information processing at the synaptic site. It was recently confirmed that there were three subtypes of glutamate receptors, and that gamma aminobutyric acid (GABA) could specifically bind to two subtypes of its receptor (one with high and another with low affinity).

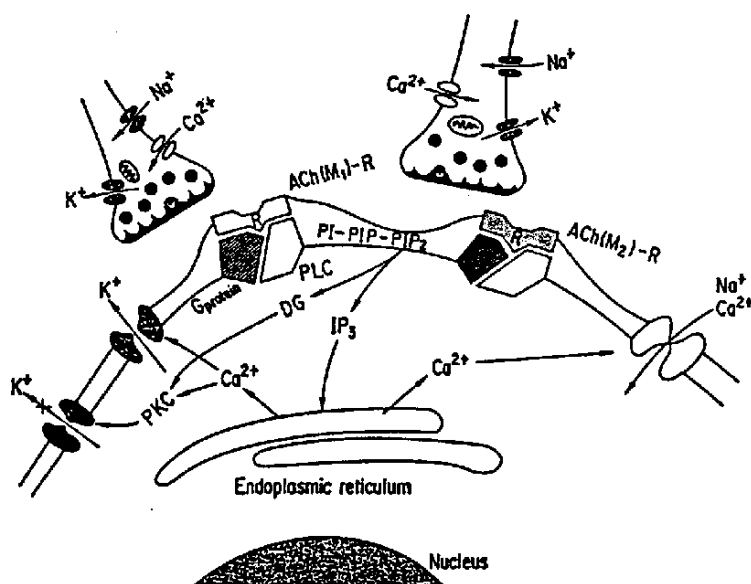What kinds of molecular mechanisms regulate the switching between

Fig.1. A schematic drawing of molecular events at the synaptic sites of muscarinic acetylcholine receptors.

depolarization (the pathway from the M_1 receptor to the K_M channel) and hyperpolarization (the pathway from the M_2 receptor to the K_{Ca} channel) on ACh application? The pathway to the K_{Ca} channel is delineated by the following molecular events which take place sequentially (Fig.1); binding of ACh to the M_2 receptor → release of inositol-1, 4, 5-triphosphate (IP_3), a hydrolysis product of the membrane lipid phosphatidylinositol biphosphate, into the cytoplasm from the plasma membrane → IP_3-induced release of Ca^{2+} from endoplasmic reticulum → opening of Ca^{2+}-dependent potassium channels. In the pathway from the M_1 receptor to the K_M channel, an enzyme termed protein kinase C (Takai *et al.*, 1982) is involved. Protein kinase C (PKC) is in the activated state only when sufficient levels of Ca^{2+} ions, phospholipid and diacylglycerol are present. Activated PKC phosphorylates and closes the K_M channel, resulting in the membrane depolarization.

In cultured CAl pyramidal neurons of the rat hippocampus, we have found that some neurons are depolarized and some are hyperpolarized when we expose them to the same concentration of ACh extracellularly (Iijima and Matsumoto, 1988). This cannot be explained by the above-mentioned difference of the ACh dissociation between the M_1 and M_2 receptors and of the fixed circuits between M_1 and K_M or between M_2 and K_{Ca}, since all the neurons tested are stimulated with the same amount (10 μM) of ACh. We have concluded that there are three types of connections between the ACh receptive site and the ionic channel in the cultured CAl pyramidal neuron, resulting in three types of differentiated neurons; the first type is the M-to-K_M type of the neuron, the second type is the M-to-K_{Ca} type, and the third type is the M-to-cation selective channel type of neuron. In the last type of neuron, ACh causes the membrane depolarization by opening the (Ca^{2+}-dependent) cation-selective channel (Fig.1).

Opening and closing of the ionic channels are regulated, directly or indirectly, by intracellular Ca^{2+} ion concentration (Fig.1). Therefore,

measurement of the regional change in Ca^{2+} ion concentration within a neuron is crucial for understanding neural information processing. This can be realized for the neuron loaded with Fura-2 (a fluorescent Ca^{2+} sensitive dye developed by Tsien *et al.*, 1985) with a SIT (silicon-intensified target) camera. The cultured CA1 pyramidal cell of the rat hippocampus is stimulated with ACh homogeneously for a period of time after it is loaded with 50 µM Fura-2 (Iijima and Matsumoto, 1988).

Rabbit Superior Cervical Ganglion Cells

Rabbit superior cervical ganglion cells all possess both nicotinic and muscarinic ACh receptors. In these cultured cells, muscarinic ACh re-sponses are found to be dose-dependent (Iijima *et al.*, 1988). In the low concentration range (<10 µM), ACh interacts specifically with the M_1 receptor and causes Ca^{2+} release from endoplasmic reticulum. Calcium ions then activate the K_{Ca} channel and cause membrane hyperpolarization (activation of the outward K current). On the other hand, in the high concentration range (>10 µM), ACh also interacts with the M_2 receptor and activates the cation selective channel, which causes membrane depolariza-tion (or the inwardly-flowing Na/Ca current). In other words, the muscranic ACh receptors respond to ACh bimodally; first excitatorily and then inhibitorily. These suggest that the sympathetic neuron becomes inactivated for a while after the neuron is exposed to high concentrations of ACh.

In the sympathetic ganglion cells intracellular Ca^{2+} ions are again crucial in regulating the ionic channel activities. In these cells intra-cellular Ca^{2+} ions are released from endoplasmic reticulum on exposure to ACh. Very recently, it has been observed that the calcium releasing sites are not homogeneously distributed but localized (Iijima *et al.*, 1988), as shown in SIT imaging of a Fura-2 loaded neuron. On the contrary, the intracellular Ca^{2+} ions homogeneously increase over the neuron on caffein application. Electron microscopic observation has indicated that the spatial distribution of rough endoplastic reticulum in a neuron is well correlated to the local sites where the Ca^{2+} ion concentration augments on exposure to ACh (Iijima *et al.*, 1988). Calcium ions may be released from rough endoplasmic reticulum on which membrane surface IP_3 receptors are concentrated.

INFORMATION STORAGE IN A NEURON

Synaptic Plasticity

Synaptic information processing undergoes constant modification by the events which take place in neighbouring synapses (heterosynaptic poten-tiation and potentiation induced by associative inputs; associative learn-ing) or by the events which have taken place previously in the identical synaptic site (homosynaptic potentiation; non-associative learning). How long the effect persists is synapse-dependent; it can last for several hundred milli-seconds to several months. The synaptic modulations are shown to be temporally divided into two kinds; (1) when the effect persists for relatively short periods of time (several 100 msec – several min) and (2) when it persists for long periods of time (several 10 min – several 10 months). The short-term modulation (plasticity) takes place in all synapses by a common mechanism characterized by an increase of transmitters released from the pre-synaptic side. It can be phenomenologically classi-fied into three classes; facilitation, augmentation and potentiation. Long-term modulation, on the other hand, has been so far observed in limited cases in cells such as the hippocampal pyramidal cells (LTP; long-term potentiation), cerebellar purkinje cells (LTD; long-term depres-sion) (Ito, 1984) and Aplysia neurons (Goelet *et al.*, 1986).

Long-term Modifications

What molecular mechanisms govern the translation of the effect of brief stimuli into relatively long-lasting molecular changes of high specificity? Recently it has been clarified that environmental stimuli can alter steady state levels of messenger RNA species encoding neurotransmitters by altering gene transcription, thereby altering synaptic, neuronal, and network function over time (Black *et al.*, 1987). Thus, brief external events can elicit long-term modifications in neuronal function. Information about the external environment is stored through the very mechanism that serves neuronal intercommunication. Multiple molecular species are available in the neuron to code for environmental events over time. As a result, the basic elements for the information storage and retrieval in a neuron are proteins, RNA and DNA while those for the processing are proteins and ions. Current opinion suggests that proto-oncogenes in the brain may represent genetic elements mediating both short- and long-term modulations in neuronal function (Hanley, 1988). Proto-oncogenes are the cellular counterparts of viral transforming genes. Therefore, we can expect that the study of carinogenesis, a process related to proliferation and tumor formation, would provide insights into the functions of neurons.

CONCLUSIONS

Neurocomputing exploits the algorithm and architecture for the information processing of neurons and neural networks to construct a computer. The basic assumption of artificial neurons on which the artificial neural networks are modelled are currently studied. We have pointed out that the assumption is oversimplified in view of the function of a real neuron. We have exemplified that the recent application of molecular and genetic approaches to the study of neural function has yielded a number of notable advances. For example, a synaptic site is a molecular processing unit that can possess a kind of memory function. The characteristics of the information processing are versatile and variable through the molecular and/or structural changes at the site. Further, contrary to traditional views, it is now well understood that single neurons use multiple transmitter signals, that different transmitters are independently expressed and regulated in the same neuron, and that experience alters gene expression in the nervous system (Black *et al.*, 1987).

These and related insights suggest that neurons should be regarded as LSI miroprocessors with a kind of memory function similar to a digital computing system. Therefore, studies on the neurocomputing should be ideally performed to address the problems as to what kind of characteristic processors are used in the brain and what kind of molecules and structures support the functioning. Then, it will become essential to determine quantitatively what the neural circuits are and what their associated neurobiological processes can do.

REFERENCES

Amari, S., 1982, Competitive and cooperative aspects in dynamics of neural excitation and self-organization, in: "Competition and Cooperation in Neural Nets", S. Amari and M.A. Arbib, eds., Springer Lecture Notes in Biomath. 45: 1.

Black, I.B., Adler, J.E., Dreyfus, C.F., Friedman, W.F., LaGamma, E.F. and Roach, A.H., 1987, Science 236: 1263.

Brown, D.A. and Adams, P.R., 1980, Nature (London) 283: 673.

Egan, T.M. and North, R.A., 1986, Nature (London) 319: 405.

Goelet, P., Castellucci, V.F., Schacher, S. and Kandel, E.R., 1986, Nature (London) 322: 419.
Hanley, M.R., 1988, Neuron 1: 175-182.
Hecht-Nielsen, R., 1986a, UCSD Extention Class Notes.
Hecht-Nielsen, R., 1986b, TRW Rancho Carmel Artificial Intelligence Center Technical Report.
Hinton, G.E., 1987, Science (Tokyo) 57: 228 (Translated into Japanese by T. Ohmori and S. Amari).
Hopfield, J.J. and Tank, D.W., 1985, Biol. Cybern. 52: 141.
Iijima, T. and Matsumoto, G., 1988, in preparation.
Iijima, T., Sekiguchi, T. and Matsumoto, G., 1988, in preparation.
Ito, M., 1984, "The Cerebellum and Neural Control", Raven Press, N.Y.
Kohonen, T., 1984, "Self-Organization and Associative Memory", Springer-Verlag, Berlin.
Matsumoto, G., 1988, Future Generations Computer Systems (in press).
Minsky, M.L. and Papert, S., 1969, "Perceptrons", MIT Press, Cambridge.
Rumelhart, D., Hinton, G. and Williams, R., 1986a, "Parallel Distributed Processing : Explorations in Microstructure of Cognition, Vol. 1: Foundations", Bradford Books/MIT Press, Cambridge.
Rumelhart, D.E., Hinton, G.E. and Williams, F.J., 1986b, Nature (London) 323: 533.
Sejnowski, T.J. and Rosenberg, C.R., 1986, Johns Hopkins Univ.Elect.Eng. and Comp.Sci.Tech.Rep. 86: 1.
Swanson, L.W., Teyler, T.J. and Thompson, R.F., 1982, Neurosci.Res.Prog. Bull. 26: 611.
Takai, Y., Kishimoto, A. and Nishizuka, Y., 1982, Calcium and phospholipid turnover as transmembrane signaling for protein phosphorylation, in: "Calcium and Cell Function, Vol. 2", W.T. Cheung, ed., Academic Press, NY, p.385.
Tsien, R.Y., Rink, T.J. and Poenie, M., 1985, Cell Calcium 6: 145.

Integrated Optoelectronics for Commmunications

C. Weyrich, Siemens Research Laboratories, Munich, FRG

The striking advantages of optical fiber communications
systems like low loss, large bandwidth and minimum cross-
talk have made fiber-optic transmission the technology of
choice for long-haul communications in recent years.
Systems operating at gigabit per second data rates and
featuring field lengths of more than 100 km are under de-
velopment or have even been implemented in the field.

Much progress in terms of performance increase and cost
reduction has been made during the last ten years. Highly
sophisticated and new structures for discrete devices,
especially for laser diodes, have been developed together
with new packaging concepts which, because of the different
material technologies involved, have to be hybride. The
transmitters and receivers devices, the various optical
components as lenses, filters, gratings or fiber pig-tails,
and electrooptic devices like modulators or switches have
to be assemmbled using micro-mechanical submounts and
sophisticated engineering tools. However, the required
accuracy of geometrical alignements of the different
components as well as the severe reliability demands limit
for the cost reduction potential.

The big challenge at present is to make fiber optics effi-
cient and cost effective for short-haul systems e.g. for
future broad band customer access connections which will be
based on bidirectional transmitter-receiver-modules or
multichannel coherent detection modules. Monolithic inte-
gration technologies can be regarded to be the most pro-
mising way for cost reduction and hence could be decisive
for the ultimate realization of customer access systems.

The monolithic integration e.g. of a bidirectional trans-
mitter-receiver-module will require the integration not
only of electronic components like transistors, capacitors,
and resistors but also of optoelectronic and optical com-
ponents like laser diodes, photodiodes, wave guides, fil-
ters or lenses. The integration of this much higher number
of functions - in comparison to purely electronic systems -
is one striking feature of integrated optoelectronic
systems.

The only materials which allow this multifunctional inte-
gration are III-V compound semiconductors like GaAlAs/GaAs
or (Ga,In)(As,P)/InP which already are base materials for
todays discrete heterostructure optoelectronic devices.
However, the basic technologies for the monolithic
optoelectronic integration of III-V-devices are not yet
sufficiently developed. Improvements of existing techno-
logies by extensive basic reasearch is needed or even new
technologies must be developed. This concernes the fields

of

- large diameter and low defect density semiinsulating substrates
- flexible and selective epitaxial growth methods
- ion implantation and diffusion processes
- structuring processes which have to be material-selective and which have to fulfil "optical" requirements

and last but not least

- design and simulation of processes, devices and circuits.

Today monolithically integrated substructures like laser-diode-transistor-driver, photodiode-FET, or wavelength division multiplexer have been realized. Their properties already reach those of hybridely integrated optimized devices. It can be expected that in the near future such devices will be used in larger quantities in optical fiber communication systems. The technological experience resulting from their production will help to further improvement of the respective technologies.

In conclusion, the successfull realisation of fully monolithically integrated bidirectional transceiver modules or coherent multichannel detection modules may possibly be a prerequisite for the introduction of optical fiber communication in the field of customer access. This should be a challenge for all researchers and engineers which are active in this field.

付録 2　ニューメディア分科会アブストラクト

CONCEPT OF PACKETIZED VIDEO TRANSMISSION OVER ATM NETWORKS

Yasuhiko Yasuda

Institute of Industrial Science

University of Tokyo

INTRODUCTION

Although ISDN has just been put into service in some countries including Japan, the next generation integrated services digital network called broadband ISDN has already intensively been studied in CCITT SG X V Ⅲ as a leading body. The broadband ISDN is intended to provide us with truly integrated services including high quality videophone, HDTV, high speed data transmission, as well as services provided by the existing narrowband ISDN.

For this purpose a single transmission and switching mode i.e. ATM (Asynchronous Transfer Mode) is to be introduced in the broadband ISDN, different from the existing narrowband ISDN which employs both circuit and packet switching modes. In the ATM network every kind of information is decomposed into constant length blocks with header called cell and these cells are statistically multiplexed and transferred at very high speed throughout the network. Since the occurrence rate of cells is permitted to be freely controlled, the ATM network can be considered to be a rate-free network from each subscriber's viewpoint.

The above mentioned property of the ATM networks is favorable in multi-media environments where the network has to deal with information sources with a variety of bitrates ranging from a few bit per second to more than 100 M bit per second and various burstiness. On the other hand it brings about a new problem especially to the field of image coding and

transmission, because image transmission techniques over constant rate networks have exclusively been studied and developed so far. This problem, packetized video, is the main subject to be discussed in this paper.

FEATURES OF PACKETIZED VIDEO COMMUNICATIONS

The features of packetized video communications are as follows :

(1) Improvement of coded image quality by variable rate coding : The variable rate coding can achieve higher coded image quality than the constant rate coding, when the average output bitrates are the same.

(2) Rate-free quality control : The variable rate coding is capable of keeping coded image quality constant, while the constant rate coding is not. The coded image quality can also be controllable according to the user's requirement in the former coding scheme.

(3) Simplification of image terminals : Simplified and lower cost terminals will be available by the variable rate coding, because it requires no large-scale memory and complicated feedback control.

(4) Possibility of new image communications : The broadband ISDN will have the capability of multi-point communication. Using this capability, it will be easy to introduce new image communications such as a kind of multi-point video conference in which each terminal has a function of editing and composing display image.

PROBLEMS OF PACKETIZED VIDEO COMMUNICATIONS

Since the concept of packetized video communications has just appeared on the stage, a lot of problems to be solved are left for their realization. Some of these are described below.

(1) Countermeasure against possible packet loss : In the ATM network it is considered that no link by link error and flow control will be

introduced. There may, therefore, occur such a case that some packets are lost due to transmission errors, overflow of common buffers, and excessive delay in buffers, even if their probability is very low. Since such packet loss causes seriously bad effect on highly compressed video signal, it is important to build in some countermeasures against packet loss. Some kinds of hierarchical coding schemes have been proposed for this purpose.

(2) To make the burstiness of coded video signals clear : In order to know the performance of statistical multiplexing in the ATM network, it is needed to make clear the burstiness property of coded video signals. Some work has been done on this matter.

(3) Rate-free quality control coding : To fully utilize the rate-free property of the ATM subscriber's channel, it is required to develop such image coding schemes that they can keep the instantaneous image quality constant and can control it to an arbitrary level. Some work has been carried out on this subject. But further study is needed, including that on evaluation criterion of image quality.

CONCLUSION

When the broadband ISDN is realized, the major information carried by it is anticipated to be video information. In other words, if image media do not become the main traffic in it, the broadband ISDN won't be realized.

The packetized video technique has recently attracted notice in relation to the broadband ISDN. However, its application is also useful to local area networks, metropolitan area networks, and private networks constructed by employing high speed digital leased lines or satellite links.

Switching Concepts for Broadband ISDN
Bernhard Schaffer
Siemens AG, Munich

Abstract

1. Network evolution

In the international discussions about Broadband ISDN it is widely agreed that the target network should be based on switching and transmission principles called "Asynchronous Transfer Modes" (ATM). This technology would allow to handle all types of information uniformly in a bitrate independent network. The long-term goal for Broadband ISDN is therefore a univeral network for all telecommunication services.

But the vision of the universal network cannot be realized in the medium term furture:

- The demand for broadband dialog services is, in the short term, for business communications e.g. LAN interconnection and this would not require a universal network.

- The existing networks will be in operation for a very long time and cannot be converted easily into a universal network.

- The idea of a universal network relies more or less on the assumption of a single network operator, but this is very questionable in a deregulated environment.

- A pure ATM network would also require a pure ATM next generation switch. Such a universal switching system would be extremely costly to develope and is very difficult to justify economically.

For these reasons an introduction scenario for Broadband ISDN is more realistic which relies on enhancements and adjuncts of existing narrowband ISDN switches and networks:

- ATM technology can be used as a flexible multiplex method to
  offer subscribers access to existing narrowband and future
  broadband networks. This is for the first step a "minimum
  integration" concept.

- ATM switching fabrics can be used to enhance STM (synchronous
  transfer mode) switches to offer ATM-connections for all
  broadband dialog services and access to existing networks.

2. ATM switches and hybrid switches
A pure ATM switch has its merits in a pure ATM environment:
all information is transported by means of cells and no
adaption is required to STM. But the use in an existing STM
environment would require adaption functions for cell assembly/
disassembly and these are not only costly but also introduce
delay in the network, which is a problem for instance with
telephony.
Another question is how to handle distributive services like TV
or HDTV:
- ATM switching for high user bitrates is quite costly and
- the merits of ATM, such as flexibility, do not play a major
  role for TV distribution.

It seems therefore very probable for the nearer future that ATM
switching will not be utilized for this purpose.
A hybrid switch could employ ATM-switching for all broadband
dialog services and STM switching for TV-distribution. For
narrowband services the existing STM switches can be used but
interworking with the ATM subscriber access has to be provided.
A possible architecture for such a hybrid arrangement is
described in the presentation.

3. Examples for STM and ATM switches
STM switching for broadband channels has achieved a good
technical performance. At Siemens, two lines of components were
developed:

- SDM switching components in bipolar technology for 32 x 16
  ports are available; a device with reduced power consumption
  for 32 x 32 ports is under development.

- TDM switching components in 1μ CMOS for 128 x 128 channels
  each 34 Mbit/s or 32 x 32 channels each 140 Mbit/s are under
  test.

In the field of ATM switching we concentrate on buffered
components. Three types of architectures were evaluated:
- Output buffers
- Centralized buffers
- Input buffers with output-oriented queue organization.

It was found out that a central buffer is advantageous if the
cell length is long (> 36 octets) whereas the input buffer
organization is preferable for short cells. In the range of
36 octets per cell both architectures show about the same data
for chip area and power consumption.
A switching matrix with input for 8 x 8 ports each carrying
140 Mbit/s buffers was developed which consists mainly of three
ECL gate arrays. A two stage array was used to built an ATM
fabric with 32 x 32 ports.

4. Field trials
A first ATM trial with the above mentioned ATM switch is planned
for the mid of 89 in the BERKOM-Project of the German Bundespost.
Here an experimental fiber network is used to gain experience
with applications of broadband communications.

Another milestone for the emerging braodband ISDN is the RACE
program of the European Community. Here Siemens cooperates with
Plessey and Italtel in a project for developing technologies for
the broadband local network (BLNT):
- A subscriber loop technology is being developed using OEIC's
  for bidirectional transmission of 155 and 622 Mbit/s.

- An ATM switch is being developed using CMOS and BICMOS for
  implementing a large fabric for transport bitrates of
  155 Mbit/s.

Further activities are planned to create a pan-European ATM
testbed for broadband services.

5. Conclusion
The universal ATM network cannot be achieved in a single step,
evolution scenarios must be taken into account which employ
hybrid approaches. The ATM network is a great challenge for
system developement and for technology, but promises a flexible
and future proof solution for the realization of Broadband ISDN.

ISDN IN JAPAN

Tetsuaki EGAWA

NTT Network Systems Development Center

Shinjuku 5-7-20, Shinjuku-ku, Tokyo 160, Japan

Separate public telecommunication networks have been constructed for each type of service, i.e., telex, telephone, and data services. Each network has also grown independently. Now, development of digital technologies has made the integration of these networks possible. Service integration will not only prove convenient for the telecommunications operating companies but also for subscribers who use more than one telecommunication service. A simple, low-price, global interface will soon allow subscribers to use any of several telecommunication services. With this kind of utility in mind, R&D has been carried out on the ISDN (Integrated Services Digital Network) over the last ten years.

The first stage of ISDN in Japan was between 1980 to 1985. During this preliminary ISDN stage, digital switching systems were introduced in Japan, and an INS Model System was constructed as an ISDN pilot project. INS stands for Information Network System. Japan has actively contributed information derived from this field trial to ISDN studies being carried out at CCITT. In 1984, I-series Recommendations were partially prepared in CCITT. The second stage of ISDN in Japan was from 1986 to 1987. Main part of the ISDN Recommendations was completed in CCITT during this period. NTT developed its commercial D70 ISDN version with a user-network interface based on the CCITT Recommendations. The third stage began from 1988. In this year, ISDN commercial services were started in the main cities of Japan. Therefore, 1988 marks the first year of actual ISDN services in Japan. Some 500 subscribers in 28 cities across the

country had entered the ISDN network by the end of September 1988.

A BRI (Basic Rate Interface) of 2B+D and a PRI (Primary Rate Interface) of 23B+D have been recommended by TTC (Telecommunication Technology Committee) in Japan based on CCITT Recommendations. A circuit switching service of 64kb/s and a packet switching service of 64kb/s or 16kb/s are supported using BRI and PRI. High speed circuit switching services of Ho (384kb/s) and H_{11}(1536kb/s) are provided using PRI. A 64kb/s circuit switching service, the first of NTT's commercial ISDN services, was provided through BRI starting in April 1988. Other services will be offered in Japan from the spring of 1989.

Figure 1 shows the configuration of the bearer network which NTT is planning. The ISDN is connected to the PSTN (Public Switched Telephone Network) and the PSPDN (Public Switched Packet Data Network). A system of local nodes will connect subscribers to integrated I-interface services. On the other hand, an individual transit network is planned for each service in order to improve efficiency. The transit network is, therefore, composed of a B-channel circuit-switched network, an H-channel circuit-switched network, and a packet-switched network. The routing operation is controlled by the local switching system.

Figure 2 shows the system configuration. A Digital Subscriber Unit (DSU) is placed in the subscriber premises. A Time Compression Multiplex (TCM) digital transmission system provides BRI through existing metallic pairs, and the optical fiber transmission system provides the PRI. The D70 ISDN version system is composed of a basic Analog Switching Module (ASM) and I-interface Sub-scriber Module (ISM). The newly-developed ISM performs the autonomous switching functions related to I-interface services. Packet calls are routed to the Packet Handler Module (PHM), and H-channel calls are routed to the H-channel switching Module (HM).

ISDN supplementary services are divided into three categories: special ISDN services, enhanced existing services, and existing services. Utilizing the

signals on the D-channel, the special ISDN services and the enhanced existing services can be given a variety of new features. Take call deflection, for example, under ISDN, a terminal will be able to change the telephone number to which a call is deflected based on the telephone number of the originating call. It will be possible to deflect a call to several telephone numbers one after another. It is not possible to provide this service through POTS because its lacks the signals containing originating telephone numbers.

Various kind of communication services will be expected through ISDN. Table 1 shows an example of these services. Narrow-band ISDN above mentioned provides digital bearer services of from 64kb/s to primary rate. Many new digital services will also emerge along with the implementation of this narrow-band ISDN. This growth will, in turn, increase the requirement for broad-band ISDN, which will provide various kinds of services up to hundreds megabits digital information. The broad-band ISDN is currently under study and is expected to be introduced in the near future.
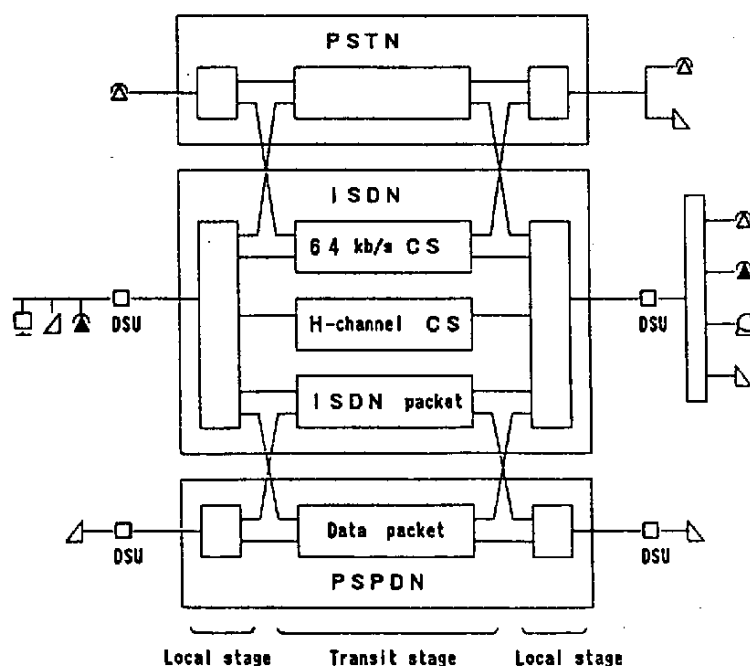
Fig. 1   INS NETWORK ARCHITECTURE

DSU : Digital Subscriber Unit
ASM : Analog Switching Module
ISM : I-Interface Subscriber Module
HM : H-channel switching Module
PHM : Packet Handler Module
STM : Supervisory and Test Module
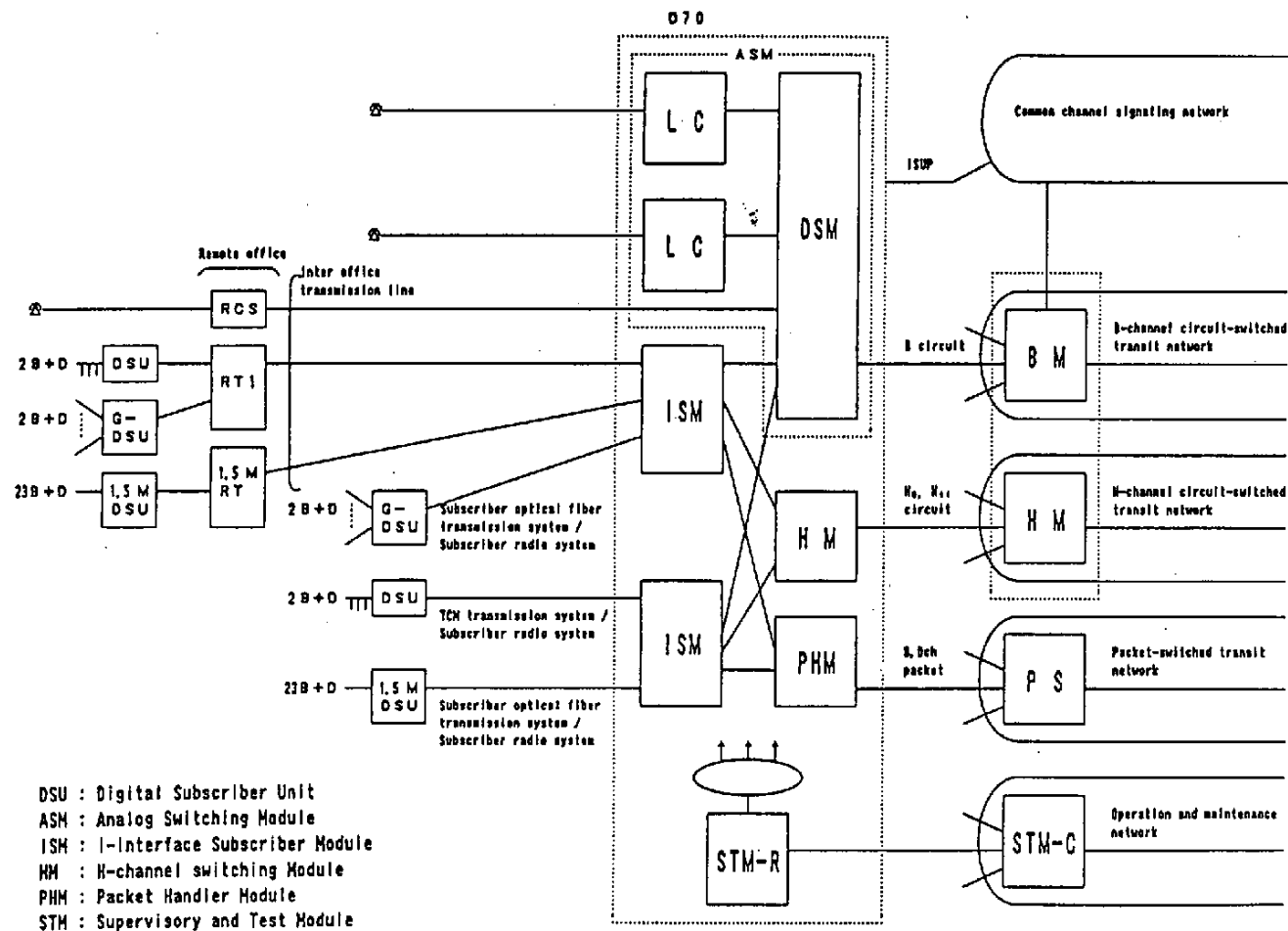
Fig. 2 BLOCK DIAGRAM OF ISDN SYSTEM STRUCTURE

TABLE 1   MULTI—MEDIA COMMUNICATION SERVICES IN NARROW—BAND AND BROAD—BAND

Media Speed		4kHz	15kHz			4MHz	20MHz
		10kbps	100kbps	1Mbps	10Mbps	100Mbps	
Continuous mass information transmission			TV Telephone · TV conference			Cable TV / Video Response System	High Definition TV
Bursted mass information transmission				CAD / CAM			
			Slow speed data transmission	LAN		File transmission	
			CAPTAIN	Still picture reference (High—definition)			
Small-quantity, multiple information transmission		Facsimile		Multipled multi—media / Multipled medium			
		Speech					

NARROW—BAND ISDN SERVICE

BROAD—BAND ISDN SERVICE

Concept of Introduction of Broadband Communication

Volker Steiner
Federal Ministry of Posts and Telecommunications

Abstract

In the Federal Republic of Germany, a highly industrialized country, broadband communications will certainly play an essential future role in many economical sectors. Yet adequate planning of networks and services is very difficult because of rather unknown demand development. Therefore the concept of introduction of broadband communications of the Deutsche Bundespost is charactericed by minimizing the risk of large advance network investment whilst providing the necessary means for early usage and service development.

The main elements of this concept as part of a general longerterm strategy to achieve Integrated Broadband Communication Network are

- phased network evolution in applying demand- and service-flexible system concepts

- strong and broad development of services and endsystemsthrough joint user - manufacturers - PTT - activities.

Important milestones in the concept implementation are the realization of the Broadband-forerunner-network (VBN), the Introduction of the "Asynchronous Transfer Mode" - switching and transmission principle and low cost local area fiber systems.

The BERKOM-Project plays a major role in creating a broad range of application pilots and terminal equipments with strong inputs to standardization as a prerequisite for large scale introduction of broadband communications.

The RACE-Program of the European Community and the newly created European Telecommunications Standards Institute will contribute on an european level to speed up the process of Technology- and Systemdevelopment as well as Standardization.

An intensive dialogue with leading countries like Japan will be necessary on all fields of broadband communications to ease the national and international Introduction.

Coherent Optical Techniques for TV Distribution in Broadband Networks

Günter Heydt

Heinrich-Hertz-Institut für Nachrichtentechnik Berlin GmbH

Broadband distribution services such as entertainment TV or HDTV for residential customers are very important for the B-ISDN. However, this fact leads to two rather different issues. On the one hand the broadband customer access has to provide for at least three TV/HDTV channels simultaneously out of a very high number of channels. Thus distribution services, which must be implemented at low costs, have a considerable influence on the complexity of the access system. On the other hand, distribution services may be a source of revenues which would allow local copper wire pair lines to be gradually replaced by optical fiber lines.

Two main technical options are currently discussed for B-ISDN implementation of TV/HDTV-distribution namely switched and unswitched broadcast.

The switched broadcast access requires only a transmission capacity which is sufficient for at least three TV/HDTV channels. The program selection is performed by a broadband switching facility in the Local Exchange which is controlled by means of signalling data sent by each TV/HDTV set and originated by the customer via his remote control device.

Unswitched broadcast systems transmit not just a few but all distributive signals simultaneously to the customers premises. The

program selection is performed by tuners located in the TV/HDTV sets. No signalling to the Local Exchange or to a Remote Unit is required.

Synchronous and Asynchronous Transfer Mode (STM, ATM) customer access systems have to employ switched broadcast whereas electrical frequency multiplex systems (Subcarrier Multiplex, SCM) and optical frequency multiplex systems (Coherent Multichannel, CMC) enable unswitched broadcast.

In the Federal Republic of Germany work on CMC systems was started in 1981 by the Heinrich-Hertz-Institute. In 1984, a first two channel system was developed and 1985 a laboratory set up of a four channel (three downstream channels and one upstream channel) customer access system was demonstrated. A ten channel TV/HDTV distribution system with nine TV channels (70 Mbit/s) and one HDTV channel (1.12 Gbit/s) was developed in 1986. This system was rather sturdily built and was demonstrated at several exhibitions such as at the German-Chinese Electronic Week 1987 in Peking.

All the aforementioned systems were operating in the optical short-wavelength region at 0.83 μm since lasers suitable for coherent communication systems were not available for the 1.3 μm or 1.55 μm range.

Meanwhile, efforts to develop CMC systems for the optical long-wavelength region have been started. This holds for the Heinrich-Hertz-Institute, where a ten channel TV/HDTV distribution system is under development and also for Europe, where the RACE program of the European Community aims at the Integrated Broadband Commu-

nication Network IBCN. One of the more than fifty projects of RACE is dedicated to the development of a CMC customer access system and to the development of specific components for CMC systems. Partners of this CMC project are Philips, Siemens, HHI, Plessey, LEP and IMEC. HHI is responsible for the frequency stabilization of the Multi-Carrier Transmitter Unit. A CMC demonstrator system is planned to be set up at Plessey for the year 1991.

RECENT PROGRESS IN OPTICAL SWITCHING

Ikutaro KOBAYASHI
NTT Communication Switching Laboratories

Many promising technologies are leading to a new generation of communication networks. Among them, optical switching has the easiest development target to describe, as its purpose is clear and its functions are relatively well defined: message signal switching in the future multimedia broadband communication network.

The history of communication switching started with electrically controlled mechanical switches. It has since experienced many structural changes. For example, first wired logic control and then stored program control were introduced to make alternate paths possible when the shortest path is busy. (In mechanical age, it was only one path uniquely determined by the dialed number.) These changes also allow more flexibility in the network design. Recent progress in switching technology has replaced the sophisticated mechanical cross-bar switches with electronic time-division switches, which deal directly with the high-speed multiplexed signals without demultiplexing.

Each new requirement stimulated the structural change, and new technologies, which timely came up, supported them. Modern requirements which drive new structural change have not yet appeared in clear form, so how should we respond to requirements for a broadband multimedia network? How should we introduce random access methods or distributed-processing into the network? It takes time to analyze these questions into technical, research, or development subjects. In any case, optical techniques(switching, frequency multiplexing, signal processing, etc.) are sure to be among the new technologies which support the change.

Optical switches have many excellent features(Fig.1). They are spread widely over the range of practicality from proven immunity to electrical induction, through the potential advantages of super-wideband optical frequency domain, which has already been demonstrated experimentally(1), to the expected high switching speeds superior to electrical switches that is still under discussion(2).

High speed channels(Gigabits per second) with immunity to electrical induction have been proved by demonstrations with optical matrix switches to be effective for small high-speed/broadband switching systems(3)(4). Before commercial

WIDE OPTICAL FREQUENCY DOMAIN·

Optical frequency

NEW MULTIPLEXING METHODS ?

F D-SW ?

FOR ROUTING ADDRESSING

RADA SYSTEM

S D-SW

T D-SW

TIME   HIGH SPEED

SPACE

APPLICATION TO ATM AND/OR PACKET ?

IMMUNITY TO ELECTRICAL INDUCTION
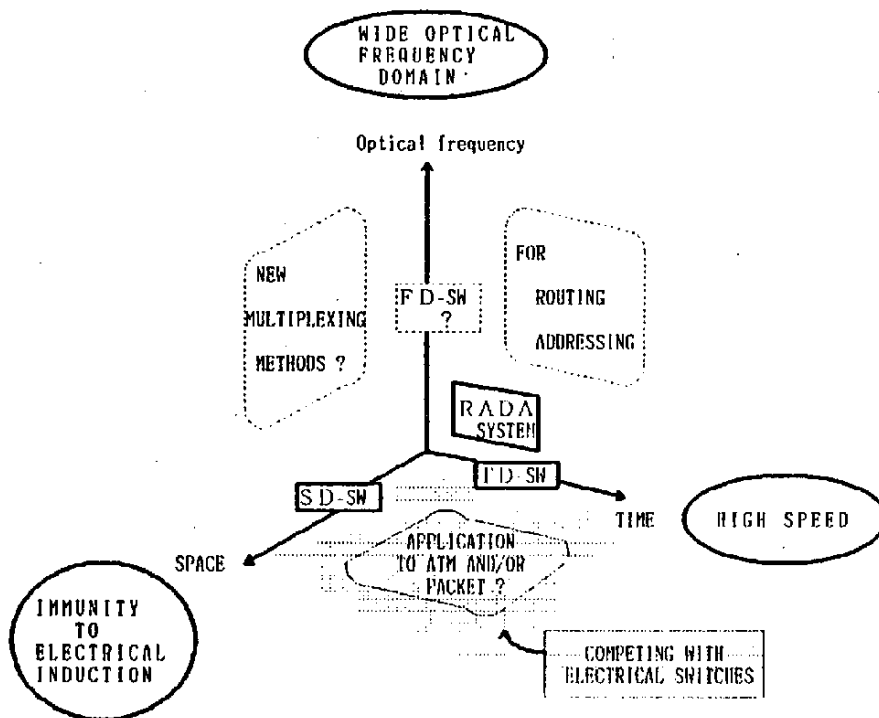
COMPETING WITH ELECTRICAL SWITCHES

Figure 1   OPTICAL SWITCHING TECHNOLOGY

use, however, the optical matrix switches have to overcome the
problems of scaling up the matrix size, removal of accidental
defects, suppression of variance in characteristics, and most
importantly, improvement of manufacturing efficiency(Fig.2).

Optical time-division switching is also expected to have a
big advantage in direct switching of time-division-multiplexed
optical signals, similar to what happened in ordinary
electrical time-division switching systems. This type of switch
has also been demonstrated experimentally(5)(4) and its
switching speed has almost reached the Gigahertz level,
although the number of multiplexed channels is less than ten,
and the indispensable optical memory and high speed optical
switch components are not mature yet. For a switching speed
superior to ordinary electrical switches, the optical-driven
photonic switch is promising; it requires no electrical driving
circuit which limits speed.
The optical frequency domain provides another dimension in
addition   to   the   space   and   time   dimensions.
Frequency-division-multiplexed signals will be efficiently
switched by frequency convertors, without need for multiplexers

and demultiplexers. Switching in the frequency domain, however, implies some difficulties or complications. Some of them would be shared by electrical switches in the frequency domain, and they were the main reasons that frequency-division switching was not applied to practical systems. For optical signals, however, there are the advantages of super-wideband and immunity to many non-linear effects like higher-order harmonics interference.

When frequency switches prove to be practical, the combination of frequency domain with space or time domain also provides wide opportunities to develop new functions for routing, addressing, and network-structures.

Figure 2   TARGET FOR PRACTICAL SWITCHING SYSTEMS

Especially, a combination of time and frequency domains promises to realize multiplexing of a large number of high-speed channels.

Although optical switches open new fields in switching system design, intrinsic superiority to ordinary electrical switches is not clear. To obtain the distinctive superiority, many techniques must be proved effective, such as parallel processing, high-speed photonic correlation, optical interconnection, and optically-controlled photonic switches.

Communication switching systems started with mechanical switches. With the change of needs and technologies, the switching circuit, including its controller, has become fully electronic. Now, the switching system seems to be on a trend toward a new structure. From the view point of promoting optical technologies(Fig.3), first, the switching circuit should be replaced by optical switches for small broadband systems, and then refined for practical use a few years later. Several years after the small-scale use, second generation optical switching systems will be designed, aiming at mass-introduction and well matched with the future network
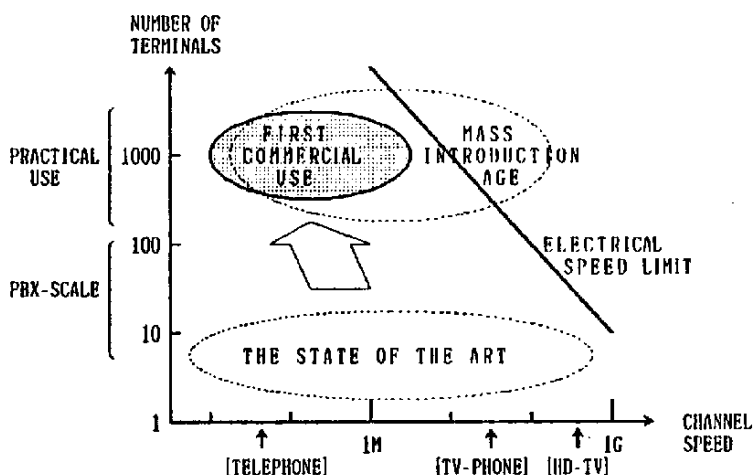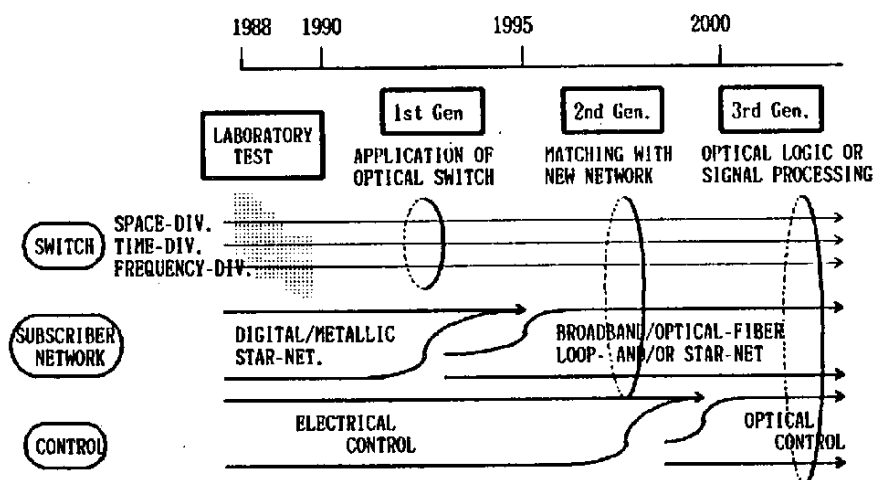
Figure 3 FUTURE TRENDS OF OPTICAL SWITCHING

structure based on random access methods and ATM technology. For the new century, optical logic circuits, optical signal processing, and optical parallel processing will play an important role in service progress as well as switching control of the third generation systems.

References
(1) H. Toba et al., Electronics Letters, Vol.14, pp.520-521, Aug. 1978.
(2) P. W. Smith, BSTJ, Vol.61, No.8, pp.1975-1993, Oct. 1982.
(3) M. Yamaguchi etal., IEICE Technical Report, Vol.88, No.129, pp.13-18, July 1988.
(4) H. Goto et al., NEC Technical Report, Vol.39, No.12, pp.138-142, 1986.
(5) S. Kuroyanagi et al., IEICE Technical Report, Vol.88, No.129, pp.1-6, July 1988.

Research and Development on

Digital Optical Processor

Dieter Jäger

Universität Münster

Institut für Angewandte Physik

D-4400 Münster, Fed. Rep. Germany

In the field of research on digital optical data processing, a first
collaborative work started in 1983/84 when the European Joint Optical
Bistability - EJOB - Project was initiated. On the German side this
programme was supported by the German Federal Minister for Research
and Technology. (BMFT) and coordinated by Haug, University of
Frankfurt. Other German partners have been the Max-Planck-Institut
für Quantenoptik München, the Fraunhofer-Institut für Physikalische
Meßtechnik Freiburg and the Universities of Duisburg, Erlangen,
Frankfurt, Hannover and Münster as associate members. The common goal
was to demonstrate a primitive optical computational device by the
end of the two years project. The German programme included research
on optical nonlinearities of semiconductors, development of bistable
devices and logic elements and study of optical computer
architectures. Results have been presented at the Hannover Fair in
1986 and are published in a report "From Optical Bistability towards
Optical Computing", North-Holland, Amsterdam 1987.

At present two national R & D programmes on digital optical
processors exist which are supported by the BMFT. These projects
represent an initiative and test phase where the main objectives are

to study the inherent potentialities of digital optical data processing. A first three years activity started in 1986. It was initiated by the Heinrich-Hertz-Institut für Nachrichtentechnik Berlin (Baack, Ihlenburg) and R & D subcontracts have been signed with the Universities of Berlin (Eichler), Braunschweig (Ebeling), München (Harth) and Münster (Jäger). In particular, optical switching and bistable devices and logic elements are currently developed on the basis of silicon and III-V and II-VI semiconductor materials. Fabry-Perot resonators and self-electrooptic effect devices (SEEDS) are investigated as well as special laser diode structures. Moreover, techniques for optical interconnects, architectures of optical parallel computers and applications in input and output units of optical processors are studied in the framework of this programme. A second programme started in 1987 at the University of Erlangen-Nürnberg (Brenner/Lohmann) concentrating on one hand on algorithms and architectures where, for example, techniques such as symbolic substitution are applied. Additionally, optical array illuminators based on phase contrast are developed as well as optical interconnects by using holographic methods. Further basic research relevant to the field of digital optical processors which should be mentioned is concerned with the theory of optical nonlinearities and instabilities in semiconductors and the realization of II-VI and III-V bistable devices at the Universities of Frankfurt (Haug) and Kaiserslauten (Klingshirn), respectively. At the University of Duisburg (Laws) concepts of optoelectronic computing networks are developed.

At the present time a subsequent joint BMFT project is being prepared

to be started in 1989/90 where several activities shall be combined in order to concentrate on future aspects and demands of optical information technology. The programme will be coordinated by Bartelt, Siemens, Erlangen. The tentative title is "Optical Signal Processing for Telecommunication". The following main topics have been proposed with special emphasis on digital signal processing. (a) Materials and technology: Silicon, II-VI, and III-V semiconductors will be important for different wavelengths. Special thin film techniques and epitaxial processes shall be developed to fabricate layered materials such as microresonators or multiple quantum wells. Technologies to fabricate dielectric mirrors and microstructurized elements will be included. (b) Device development: Nonlinear Fabry-Perot resonators, passive and active hybrid devices and alternative switching concepts, e.g. in gratings, shall be studied. A key subject will be the realization of two-dimensional arrays of switching and logic elements. (c) Optical interconnects: Here classical concepts as well as random interconnects are of interest. Microoptic and holographic optical elements will be considered but also fiber connections. (d) Light sources: Special aspects of device control by semiconductor or other conventional lasers shall be investigated where beam forming and array generation techniques play a key role. (e) Input and output units: Spatial light modulators and arrays of optoelectronic conversion elements are foreseen to have special applications. (f) Optical systems and architectures: Here optically controlled optical switching networks and also optical processors and computers are of interest where suitable architectures have to be developed. Neural networks may offer interesting concepts for special applications. (g) Applications: Possible areas of short- and long-term applications have to be analysed.

Optical Information Processing

Satoshi ISHIHARA*

Optoelectronic Industry and Technology Development Association (OITDA)

20th Mori Bldg., 7-4, Nishi Shimbashi 2-chome, Minato-ku, Tokyo 105, Japan

Abstract

As the recent advancement of the intelligent society has accompanied an increase of information, requirement of handling a large amount of information at a high speed rate in an unconventional manner has become increased. For processing such information, light can provide suitable means due to many useful characteristics including :

1) high bandwidth,

2) massive parallelism,

3) availability of multiplexing : wavelength, polarization, etc.,

4) freedom from detrimental coupling effects.

*) permanent address : Optical Information Section, Electrotechnical Laboratory, 1-1 Umezono, Tsukuba City 305, Japan

The function of a generalized information processing system is illustrated in Figure 1. The above characteristics enable light to be applied to each subordinate functions in the Figure. Actually, according to the survey by OITDA as shown in Figure 2, the output of optoelectronic products in 1987 in Japan is over 1.2 trillion yen, where 90% of them corresponds to those products whose function can be found in the Figure 1. Most of them forms the surrounding part of the Figure 1; e.g. 30% corresponds to the lower part, namely, optical communication, at present. Thus, it is quite natural to utilize light in 'Information processing' illustrated in the center of the Figure 1, as well.

Optical information processing in a narrow sense, or optical computing in other words, has recently drawn many approaches for research and development. One of the reasons for such growing attention is considered to be the requirement from the users (the intelligent society) as stated above. However, the development of optoelectronic technology, especially the development of many devices, including the reliability improvement and the price reduction, can not be neglected.
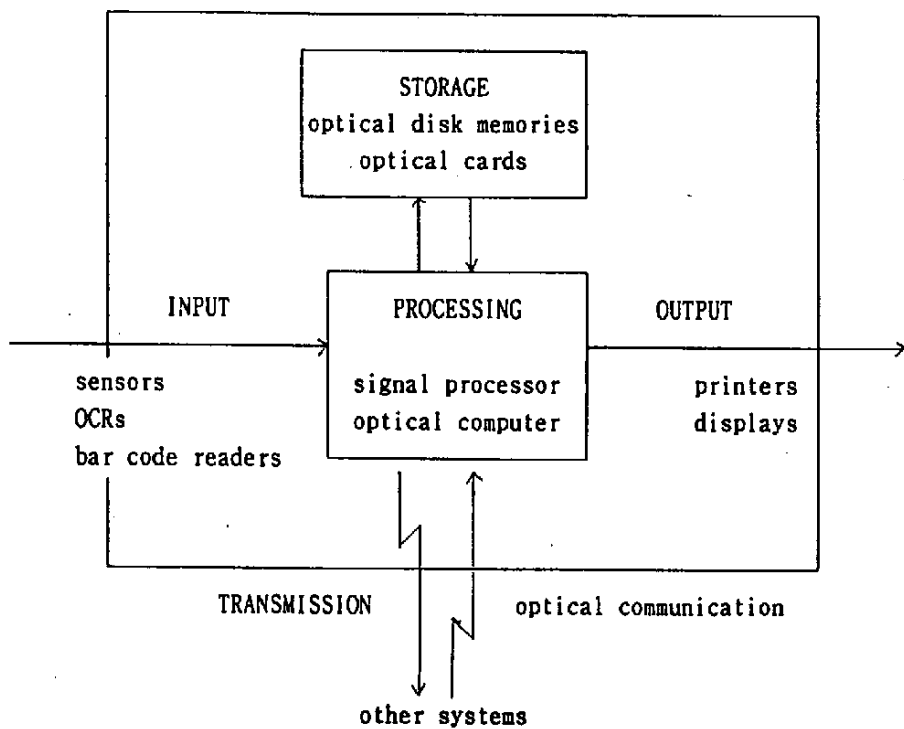
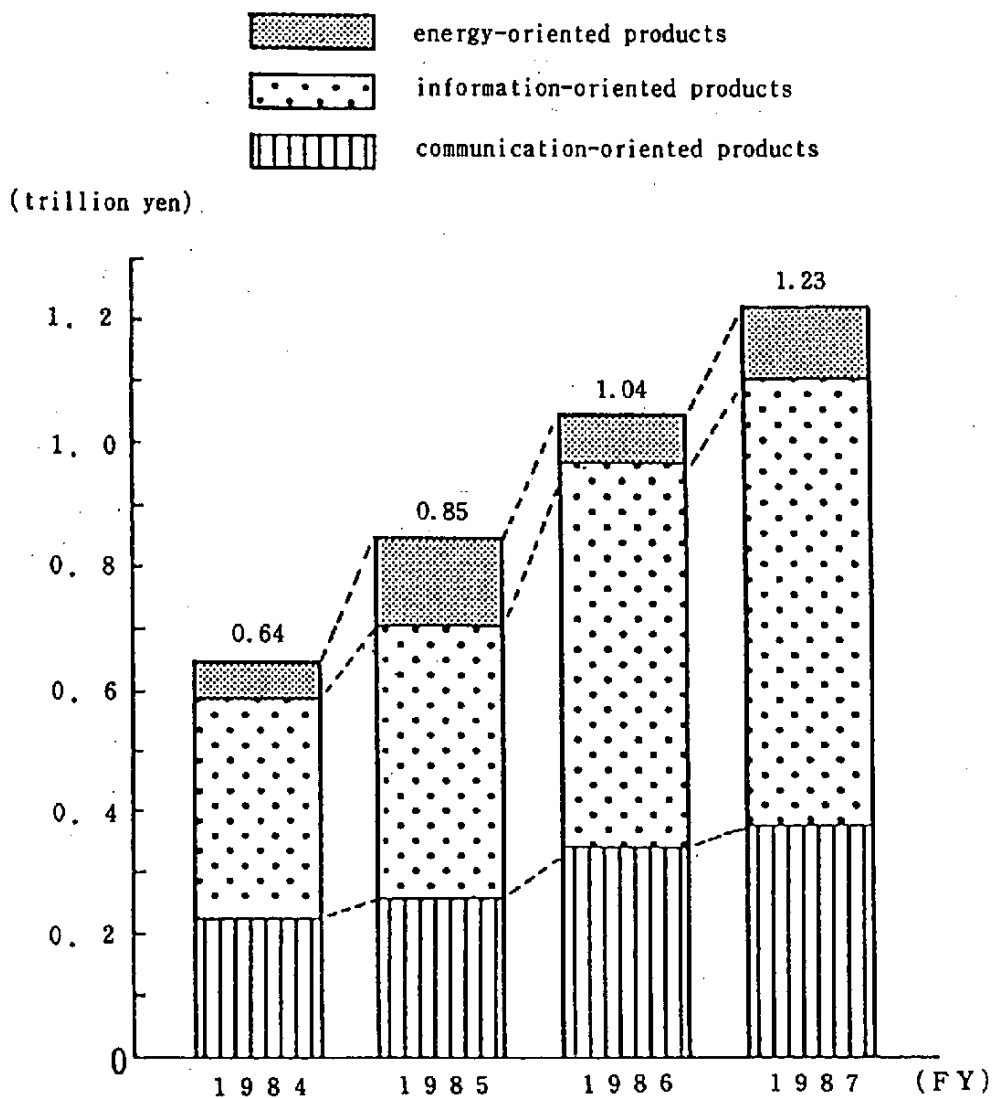Figure 1 : Generalized information processing system and some application with light

Figure 2 : Optoelectronic products in Japan

Optical Switching, State of The Art

Günter Heydt

Heinrich-Hertz-Institut für Nachrichtentechnik Berlin GmbH

At present, the importance of optical switching for the B-ISDN is not clear. This is certainly due to the fact that microelectronics are highly developed and thus high performance electronic broadband switches are already available whereas optical switching means are in a rather early stage. However, it seems to be possible today to assess the future role of the main principles of optical switching for B-ISDN applications.

The optical switches reported most frequently are of the switched waveguide type, realized on Lithiumniobate but also on semiconductor materials. Generally, these coplanar optical switches require direct electrical control of each crosspoint. The number of inputs and outputs is limited to rather low numbers and the interconnection of submatrices in order to achieve switching networks with high numbers of inputs and outputs is quite difficult. It is today not conceivable that these switches will compete successfully with electronic B-ISDN switching networks, but there may be special applications, e.g. for Inhouse systems.

Another principle of optical switching employs an optical frequency multiplex. Each input fiber is fed by an optical carrier frequency comb, each carrier is modulated. The switching elements select one of the carriers an transfer the modulation to another carrier of the output carrier comb (non Fig.). The realization of such a switching element can be performed by the combination of an

optical heterodyne receiver and a coherent transmitter module. Provided that a monolithical integration of these TR elements is possible, this coherent multichannel switching can be an interesting solution for the B-ISDN since the TR elements perform not only the switching but also regeneration and amplification.

The division Integrated Optics of the Heinrich-Hertz-Institute has developed in 1986 4x4 Lithiumniobate Submatrices which were cascaded exemplarily to a 16x16 switching array. This optical switch was employed within an Inhouse communication system (LOCNET) for switching of videophone signals with a bit rate of 70 Mbit/s. The system showed a good performance but also the technical limits of such switches.

Additionally, first experiments in the field of coherent multichannel switching have been performed 1987 at the Heinrich-Hertz-Institute. Optical heterodyne receivers and coherent transmitters were connected via an optical star coupler. The optical frequency of these elements was controlled by means of a computer and the switching function was successfully demonstrated.
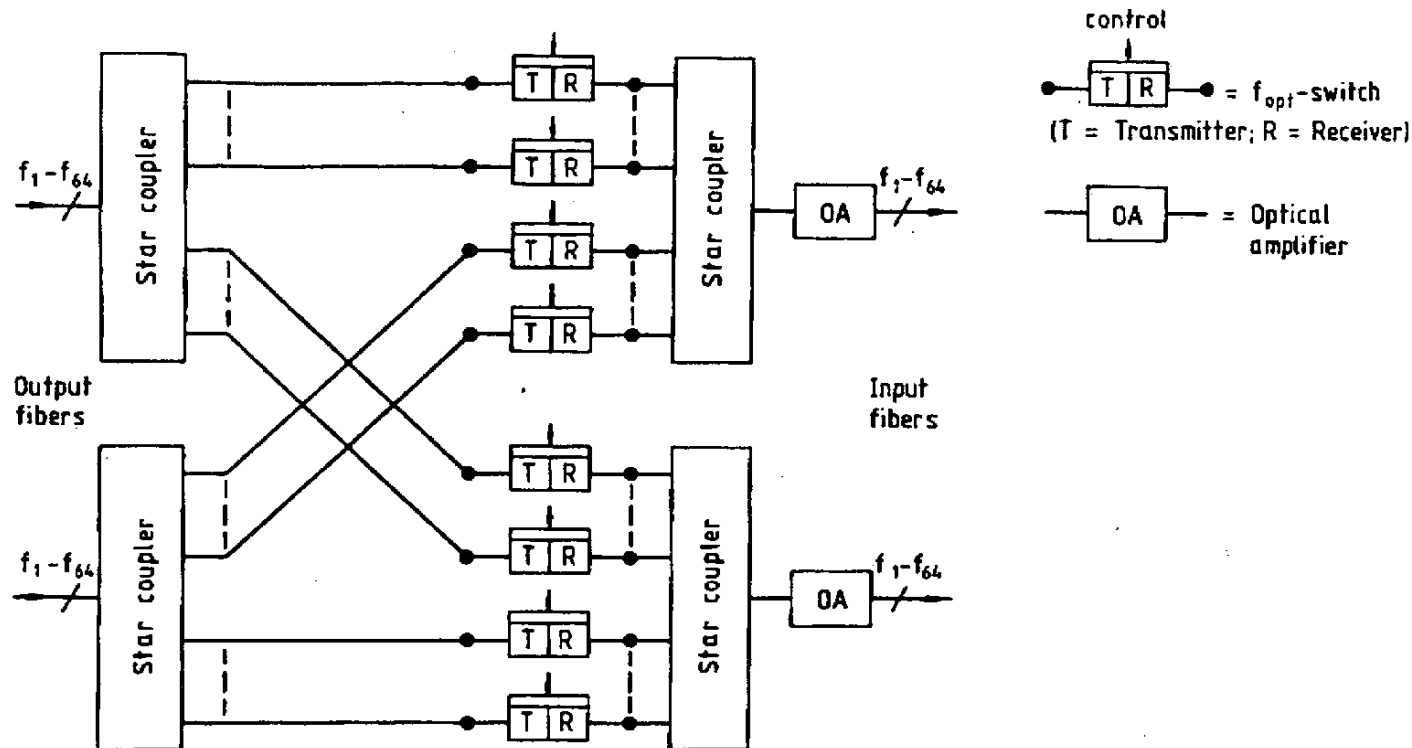
Optical Frequency Switching Network

OPTICAL PARALLEL DIGITAL COMPUTERS

Yoshiki Ichioka
Department of Applied Physics, Faculty of Engineering,
Osaka University, Suita, Osaka, Japan

Studies on optical computers have been categorized to three streams,
i.e., those on 1) opto-electronic computers, 2) optical parallel
computers and 3) optical neural computers. An Optical parallel digital
computer is a massively parallel computer which makes good use of
features of parallel information transmission and processing in light
wave and of flexibility in digitral processing.

In this review, the new optical parallel digital computing principle-
optical array logic--developed in our laboratory is described, and the
architectures of the Optical Parallel Logic Array System (OPALS)[1-4]
designed using the principle of optical array logic are demonstrated.

The OPALS is a kind of parallel optical digital computing system. Its
salielent features are the capability of implementing fully 2-D parallel
logical operation, and parallel neighborhood operation, programmability,
capability of iterative processing, and separability into modules.

Optical array logic is a technique to implement any parrallel
neighborhood operation using techniques of image coding, 2-D correlation,
sampling, and logical sum. Optical array logic can achieve parallel
neighborhood logical operation, or cellular logic for 2-D binary images.
In optical array logic, the method of optical parallel logic gates
developed in our laboratory is employed.

Figure 1 shows the processing procedures of optical array logic.
Its processing principle is the same as that of array logic in
electronics except for the parallelism. Two binary input images
consisting of N×N pixels are spatially coded and converted into a coded
image. N^2 logical operations are concurrently executed for a coded
image. An operation for the specific pixel is expressed by the logical
sum of several product terms and by a product term operation and OR
operation. A product term operation is carried out by 2-D correlation
of a coded image and an operation kernel followed by a coding process.
The decoding process consists of spatial sampling and thresholding.
The parallel OR operation for the decoded signals provides the result of
the given operation. In optical array logic, the type of an operation
is determined by the combination of operation kernels selected.

Optical array logic is a technique implementing parallel processing
of two input and one output 2-D signals. Feeding the output signal

back to the input part as one of the input signals in the following
steps of operation makes it possible to execute iterative processing.
The OPALS is the system capable of implementing these operations.
Figure 2 shows the schematic diagram of the OPALS.

We have considered several realizable versions of OPALS's. They are
1) electo-optical version of OPALS   2) all optical version of OPALS,
3) modularized OPALS and 4) birefringent OPALS.   Either system is
composed, centering on a loop processor.

In the electro-optical version of OPALS, encoding of input signals,
processing of output signals, and feedbacking of an intermediate
processed result are performed by electronic techniques.

In the all optical version of OPALS, a dynamic coding method using
spatial light modulators and a dynamic optical correlation technique
using a multi-focus imaging system are utilized.   The 2-D S-R type flip-
flop and D type flip-flop to be developed in future are required to
excecute the sequence of product term operations or to carry out
iterative processing.

The modularized OPALS can be constructed from several functional
modules : mixing/distributing, encoding, correlation, and decoding
modules.   The encoding module is opto-electronic devices integrating PDs
and LEDs for pixel-divided processing, which can be fabricated by LSI
technology.   2-D array of pixel processing elements is easily composed by
increasing the number of the element module.   The correlation module
executes the real-time 2-D correlation for optical array logic.

The birefringent OPALS is a kind of all optical version of OPALS
using the princeple of the birefringent encoding.   The birefringent
encoding is a parallel and space-variant image coding method.
Advantages of birefringent encoding are simplecity,stability, parallel
nature, and light power efficiency.

We have already constructed experimental systems of the electro-
optical version of OPALS and the birefringent OPALS.

On the OPALS, operations for parallel processing are programmed in
optical array logic and the program can be optically carried out.   This
programmability proves usefulness of the OPALS. Some experimental results
implemented on the OPALS are demonstrated.

References
1. J.Tanida and Y.Ichioka,   Appl.Opt. 25,1565 (1986).
2. J.Tanida and Y.Ichioka,   Appl. Opt. 25, 3751 (1986).
3. J.Tanida and Y.Ichioka,   Appl. Opt. 26, 3954 (1987).
4. J.Tanida and Y.Ichioka, "Birefringent optical logic processor,"
   in Technical Digest, XVI International Conference on Quantum
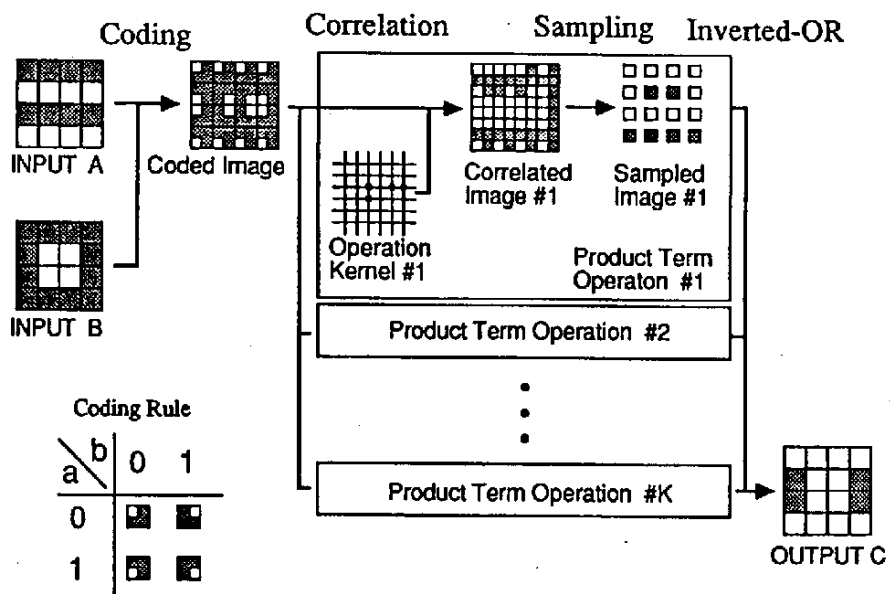   Electronics, Tokyo (July 1988).
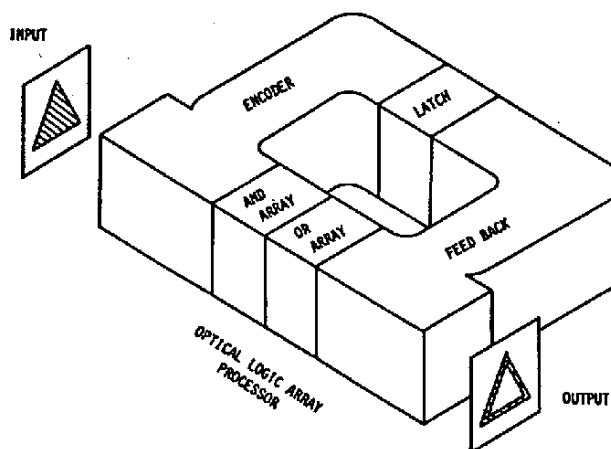
Fig.1 prosessing procedures of optical array logic

Fig.2 Schematic diagram of the OPALS

SOCIAL ACCEPTANCE AND SECURITY PROBLEMS OF
NEW INFORMATION SOCIETY

T. Uezono

IBM Japan Ltd.

I.   Summary of Current Status

Transformation from Industrial society to Information society is currently be-
ing proceeded in leading countries. As an indication of this situation, "Centra-
lization" and "Distribution", seemingly a contrdicting phenomenon, is proceeded
at the same time. That is to say, Polarization of information to Tokyo is taking
place without suppression.

On the other hand, some functions which can not be handled by centralization,
are passed to local area. The distribution spreads even to overseas countries.
For example, subcontract production of software in Asian developing countries
(NIES) is said to be increasing.

Global network shortens distance and time differences among countries. At the
same time, it changes Tokyo into a center of information exchanges.

To support and promote such phenomena, followings are noted;
   1. New and various kind of medias are required. And those medias are being
      invented continuously.
   2. Information systems are becoming larger in size, higher in speed, more
      automated and more popular.
Subsequent to the above, it is unfortunate to note that the computer abuse is
not limited to a certain countries only.

II.   Problems

The biggest problem of all is that below listed events do not match the promo-
tion and technological advances of the above said facts.
   Those events namely are;
   1. Ethics or way of thinking toward information
   2. Business practices in information age

3. Legal systems in information age

4. Indemnity insurance systems in information age

5. Security measures in information age

In Japan, new things have been relatively welcomed. In other words, Japanese have had higher social acceptance towards new technologies and medias. Japan's fast economical growth in past several ten years and its optimistic thinking are the reasons for such an acceptance.   To obtain continued and fast economical growth, Japan had to create new products fast and cheap which has led to accept new technologies and medias easily.

On the other hand, Japanese are insensible to security thinking that ' Water and Security are free '.   A foreigner has warned that such optimistic thinking may be dangerous.

Thus, whether Japanese society accepts a sophisticated informatization or not may not be an issue, but too lax acceptance itself may be an issue.   It is my observation, but in Europe and the United States, information security, privacy protection and other countermeasures have been provided to get social acceptance for informatization.   In Japan, those countermeasures are rather needed not to disappoint Japanese society's expectations toward new medias (which are preceded than the real change).

III. Will above said situation continue in Japan ?

Are these optimistic view going to continue ?   When bicycle is on a run, it does not fall. When society is growing, the growth itself provides security. If so, when Japan becomes matured society, security will play an indispensable role.

And such symptom is showing. As Murphy's law says, "If something can be wrong, it will certainly go wrong at sometimes or other".

Let us go back to five facts mentioned before.

1. Ethics or way of thinking toward information
   According to the survey done by Police Agency in 1987, people's feeling towards 'information handling' cannot be regulated by conventional moral toward handling of 'object' such as money.

2. Changes in business practices

   With the promotion of communication network, VAN, POS, etc., Japan's tradi-
   tional wholesale dealer system has been collapsed. In turn, agency business
   (taking over part of jobs in enterprises by providing value added informa-
   tion) is prospering.

3. Legal systems in information age.

   Criminal Law of Japan which was amended in 1987 has counteracted against
   computer crime. However, it is not sufficient.

   For example, according to Japan's criminal law, huckers who hucks into
   other's computer system for fun, are not punished.

   Personal information protection law is still not legalized yet in Japan.

4. Indemnity insurance systems in information age

   There are two indemnity insurances against information processing related
   loss, but not well sold. One of the reasons for these insurances not get-
   ting very popular is that unlike the money value, information value cannot
   be measured with standard measurement system.   When we cannot convert
   information value into monetary value, insurance cannot cover the loss.

5. Security measures in information age

   Countermeasures for physical security are being taken in Japan, but for
   logical security, countermeasures are not sufficient due to probably Japa-
   nese optimistic way of thinking. In addition, security measure is tend to
   be considered as a subject of technical engineering. But, it should be dis-
   cussed from legal, socio-psychological and management engineering aspects.

IV.   Conclusion

What considerations are required to help our society grow to really acceptable
information society ?

   1. Awareness of Researchers and developers

      Researchers and developers of leading-edge technology should pay more at-
      tention to the impacts that his outcome bring to the society (especially
      that of negative impacts). It is easy to say this way but hard to practice.
      Because, mankind has never acquired such 'Predictability' like God has.

   2. Necessity of preventive medicine to such problems

      Taking preventive action is a minimum requirement against such impacts, if

anticipating social impacts of the leading-edge technology is difficult.

   i. EDP Audit or Systems Audit is one of the preventive actions.

   ii. It is mandatory to establish security policy in a society and amend procedures periodically.

   iii. Computer Virus is serious problem.   To prevent the plague from spreading, the original vendor of software may need to announce "Declaration of Sanitization" on his software , modelling after the public hygiene.

3. Establishment of information value measurement system

Counterfeit and poisoning of water supply are heavily punished legally due to strong impacts such actions give to the social security and discipline. With the same consideration, a more heavy punishment to the counterfeiting or intentional transformation of information would be required by society. To conform to the requirement, it will be necessary to establish standard measurement system for information.

Note. The opinion herein is author's and does not represent the opinion of the organization he belongs.

INFORMATION SECURITY IN NEW MEDIA

Klaus D. Wolfenstetter

Research Institute of the Deutsche Bundespost

ABSTRACT

It is a matter of fact that an integration of security services into telecommunication and information processing services is becoming increasingly important for a number of reasons. We find the necessity for security features in nearly all telecommunications technologies including local area networks and personal computers, distributed databases, cellular radio telephones, satellite teleconferencing, electronic mail and funds transfer. In connection with recent deregulatory trends in communications laws this has set off a revolution in communications security.

Today vast amounts of sensitive information such as health and legal records, financial transactions, credit ratings and the like are routinely exchanged between computers via public communication facilities.

These are all examples of communication services in the private and commercial business sector and do not concern the military and diplomatic communications.

So the beginning "Information Age" has revealed an urgent need for cryptography in the private sector. Worldwide open research in cryptology has, in fact, taken place only for about the last ten years.

On the other hand, most people engaged in communications technologies agree that only a worldwide open systems interconnection can meet the demand for efficient and economical communication services. Thus, we have to combine openess with security or (better:) confidentiality. In this context, confidentiality need not impede the development of open systems, it is rather a prerequisite of their success. It is true that the two features "open" and "secure" seem to exclude each other, but these two goals can be achieved by means of public key cryptography.

Furthermore many security problems such as key management, message and person authenticity, anonymity, etc. can be solved elegantly by using such tools.

The enormous growth in research in all aspects of modern cryptology involves a variety of theoretical and practical problems, such as

- classification of security lacks and services

- development of security schemes and protocols

- development of security algorithms

- assessment of the computational complexity of functions and algorithms

- problems in number theory and algebra and related coding theory

- embedding security related features in system environment

- problems concerning IC card and security module technology

The paper deals with some of these problems, which are outlined in an increasing degree of complexity, ranging from straightforward cryptographic schemes to demanding multifunctional security systems. In parallel, some typical applications in telecommunication services are given.

Electronic Signature as an Add On to the Teletex Service

Wolfgang Schroeder

mbp Software & Systems GmbH

Semerteichstr.47-49

D-4600 DORTMUND

In the next decade the developed information society will strongly benefit from the fast growing potential of digital electronic communication. But at the same time new threats and risks will grow with these new communication features, equally for individuals and commercial oriented or public organisations; while in the *private* sector protection of privacy is the most desirable good, in the *public* domain the value of digital communication will strongly depend on social acceptance and legal evidence in our communities and business organisations.

When we concentrate on this latter aspects and on the various kinds of electronic message transfer, we are exposed to several risks resulting from the use of an electronic transfer system. While a *reliable* exchange of arbitrary text or data information is state of the art in modern communication even between different types of computers (OSI concepts), all these technologies cannot guarantee a *trustworthy operation* of the total electronic message exchange system. Main threats today are still the risks of

- *Masquerade* (somebody pretends to be someone else by using a wrong authors name in a message)
- *Repudiation* (somebody denies to be the author of a message after having sent the message)
- *Manipulation* (somebody changes the contents of a document after electronic reception or transmission)

- *Interception* (an unauthorized person intercepts a message during electronic transmission)
- *Disclosure* (an unauthorized person gains access to the contents of a non-public message)

To overcome these potentials in order to achieve trustworthy and hence legally binding electronic communications, mbp Software & Systems and the GMD (Gesellschaft für Mathematik und Datenverarbeitung) have closely cooperated to develop a fully operational add-on system for the international Teletex service. This electronic document transfer service was selected as one of the most suitable types of message exchange in an open systems environment. Although based now on mbp's line of UTC Teletex controllers and TELETEX-PACK software providing Teletex access to PCs and other office computer systems, the concept itself is as well independent of the specific type of terminal as not restricted to upward compatibility.

The pilot-product developed by mbp and GMD overcomes the above mentioned threats by providing two independent security services:

- a *Signature-Service* (protecting against masquerade, repudiation and manipulation) and
- a *Confidentiality-Service* (protecting against interception and disclosure)

The concept is based on an intelligent microprocessor based chipcard. The card, individually assigned to the card-holder, carries a unique pair of keys to be used with the asymetric RSA encryption algorithm. The access to these keys stored in the non-volatile memory of the card is protected by a fully user controlled PIN

(PIN = Personal Identification Name). In addition, the card holds
a validation certificate (or a hirarchy of certificates) of the
issuing organization and/or trustworthy authority.

Signing a document with the chip-card requires that the author
identifies him/herself by showing to be the legal owner of the
used chip-card entering the correct PIN-code. TELETEXT-CRYPT will
then perform a mathematical folding procedure (Hash function) re-
sulting in a checksum which in the end is transformed by applying
to it the RSA algorithm using the secret key of the card-holder.
The "electronic signature" as the result of the process is presen-
ted on an appended signature page of the Teletex document showing
author, signature and validation certificate in man (and machine)
readable ASCII (see below).

```
2627-23136911-nbpUTC    /2627-6141947-GHDTX    /86-08-16-10:34/612-601

nbp Software & Systems GmbH               Dortmund, 16.3.1988
Dr. Wolfgang Sohröder
Semperteichstr. 47-49
4600 Dortmund


GHD
Herrn Bruno Struif
Rheinstr. 71
6100 Darmstadt


Sehr geehrter Herr Struif

Wie in dem telefonischen Gespräch am 15.3. mit uns
vereinbart, möchte ich Ihnen hum noch einmal schrif
daß wir hiermit verbindlich die Abnahme der unter P
7.993.5623.445 von Ihnen erbrachten Leistungen erkl

In der Hoffnung auf eine weiterhin gute Zusammenarb

mit freundlichen Grüßen Ihr

Wolfgang Sohröder
```

```
2627-23136911-nbpUTC    /2627-6151947-GHDTX    /88-05-16-10:34/612-002

*******************  T E L E T E X - C R Y P T  ********************
*                                                                  *
*    Electronic signature by / Elektronische Unterschrift von      *
*                                                                  *
*    ORG: Dr. Wolfgang schroeder / nbp Software & Systems GmbH     *
*    VAL: 88-03-17 : 90-03-17                                      *
*                                                                  *
********************************************************************

PAR: V-RSA1.0 /34
SIG: AEMCOGNUE:INDIOCKJDNADIABIBRGNACCJCKCKIPNNDFLDOLKCNPFPPALC:AEKTCN
     INQ
KEY: JUSLPHPDKFCHINFNGZGLOCLICLIPKBGPFDGBJCBPEF?FNFHJALOCGPJLFPDFBAAA
     AAPQ
VAL: 88-03-17 : 90-03-17
ORG: Dr. Wolfgang schroeder / nbp Software & Systems GmbH
     Semperteichstr. 47-49 , D-4600 Dortmund 1


PAR: V-RSA1.0/44
SIG: ELMJNBANHXPFCULJFYSDARELZAJNDRCHKJHOFGIKDBAXPALNHDCLIGKOJPKGJCLJ
     CKHFXACODLNLCCNKIGLBQ
KEY: FGAJLNKCFKOIUNCFPFHNCNASPOLFBGPDFIBNGNCGPLKFDJDKKAFNGGNGPFGRPKGN
     BBANCCBIISNGFFCAAAAABQ
VAL: 88-03-17 : 90-03-17
CTA: nbp - Dortmund   Software & Systems GmbH
```

To allow the receiver to check and prove authorship and integrity of the document, the public key of the author is provided in addition on the signature page. By applying the same Hash-function to the text and using the delivered public key, the receiver of the message can easily check the authenticity of the document. This validation function is performed automatically, whenever a signed document is retrieved by a user from the Teletex receive memory of the controller or can be initiated by the operator any time later after storage in the local filing system.

Similar to the electronic signature an optional encryption is performed by using the *public key of the receiver*: Only the addressed individual, i.e. the legal card-holder will be able to decrypt and read the received encrypted document. An additional not-encrypted header page is automatically created to clearly identify the addressed person and a subject reference in plain text. The key-management problem arising from the encryption feature is solved in TELETEX-CRYPT by a local "public-key database" of the communication partners of a specific user.

Data Broadcasting

Akio Yanagimachi

NHK Science and Technical Research Laboratories, Tokyo

1. Introduction

Broadcasting has steadily progressed, starting from AM radio, then advancing to black and white television, FM radio and color television, and now to the development of high-definition television (HDTV). In addition to these sound and image broadcasts, we now have another quite new broadcasting conception, that is, data broadcasting. Data broadcasting is a service to transmit coded information to the data processor (e.g. personal computer) possessed by a subscriber. This service will play a significant role for individuals who will increasingly need information in many phases of their lives.

2. Developing Data Broadcasting Channels
2.1 Multiplexing on Sound or Television Broadcasting

Radio program identification codes can be transmitted by multiplexing low bit rate data on AM broadcast waves. This method transmits data having a 16 bit/sec rate by continuous-phase frequency-shift keying with 24 Hz and 32 Hz signal frequencies. Carrier waves are modulated either by amplitude or phase.

FM stereo broadcasting can add a subcarrier above the subchannel spectrum and modulate the subcarrier by QPSK, for data transmission. This method has been put to field use to send to stationary receivers 32 Kbps of ADPCM sound and 1 Kbps of data.

A newly developed method multiplexes a digital subcarrier above the subchannel of terrestrial television sound that is frequency-modulated, as done in FM multiplexing, for transmitting facsimile signals.

Satellite TV broadcasting operates two-channel transmission by a digital subcarrier NTSC system. The subcarrier is multiplexed on a 5.73 MHz video signal band for QPSK transmission of sound and data at a rate of 2.048 Mbps.

The data transmission uses remaining bits of sound transmission. The capacity of data transmission may differ over a range between 224 to 1,760 Kbps by the mode and number of channels of transmitted sound.

The method originally developed for teletext multiplexes non-return to zero (NRZ) data signals on free scanning lines in vertical blanking intervals of television video signals. The data signals are multiplexed at a rate of 296 bits on one scanning line per field, producing a transmitting capacity of about 16 Kbps. Teletext currently uses four lines in this method for operational services.

2.2 Exclusive Channels

This method exclusively uses one channel of TV broadcast waves in two ways: one using all lines of video signals to transmit NRZ signals as Teletext does, and the other employing an exclusive digital modulation method. The NHK is studying digitally modulated wave broadcasting which uses a 27 MHz band of one satellite broadcasting channel. It can send 12 units of 2,048 Kbps, equivalent to the capacity of the said satellite TV sound multiplexing.

Table 1 summarizes various data broadcasting channels described.

3. Developing Data Broadcasting Services

Data broadcasting is no different from radio and television services in that it eventually conveys information to the receiver, but they differ in the ways the receiver processes coded information.

The following are representative data transmitting service media now being developed:

3.1 Facsimile Broadcasting

Prints out detailed information on paper, using MH codes based on the CCITT G3 format now widely used for telefacsimile services. High-speed transmission is possible via data channel of satellite broadcasting. Transmits an A4 size in 20 to 30 seconds on a printer with a maximum scanning line time

of 5 ms. Transmitting half tone, which is inevitable in facsimile service, can be coped with by the dither method. The data channel of satellite broadcasting uses a packet transmission system. This system, when transmission completes within the minimum scanning line time, restricts packet transmission for higher total efficiency.

3.2 Personal Computer Services

These services provide the transmission of personal computer programs and broadcasting of various data to be processed and shown on a personal computer display. The programs include CAI (computer-assisted instruction) and TV games, while the data services convey weather data and economic indexes. The programs and data can be stored in the receiver's computer for later convenience.

3.3 "Telemusic"

There is an increasing number of musical instruments on the market that electronically generate sound or electrically input/output performances through an automatic piano. "Telemusic" broadcasts performance data to these instruments. This method needs far less transmission capacity than the conventional system that transmits signal waveforms of the sound pressure caught by the microphone and reproduces them on the receiver's speaker. Also, this method provides vivid sounds of real musical instruments.

Transmitted performance information includes sound pitch, intensity, duration and timing, which are exactly matched to actual playing.

4. Future Prospects

The satellite data channel and exclusive wave digital broadcasting have a large transmission capacity and the flexibility of the packet transmission system which can simultaneously broadcast various kinds of information. This enables the information sender to use several media simultaneously and the receiver to select and get necessary information quite easily. Data

broadcasting will develop into ISDB (integrated services digital broadcasting),
a system to transmit any kind of information perfectly.

Table 1 Various data broadcasting channels

Type of data transmission	Frequency band & modulation of main carrier	Data multiplexing & modulation	Data bit rate
Multiplexed transmission with main program	Medium wave AM (sound)	Double modulation of main carrier CP FSK	16bps
	VHF FM (sound)	Subcarrier (76KHz) QPSK	1Kbps (48Kbps)**
	VHF/UHF FM (TV sound)	Subcarrier (70.8KHz) QPSK	16Kbps
	SHF* FM (TV video)	Subcarrier (5.73MHz) QPSK	224 – 1760Kbps (2,048Kbps)**
	VHF/UHF/SHF* AM/FM* (TV video)	TDM (VBI) NRZ (5.73Mbps)	16$\times$n Kbps
Exclusive channel transmission	SHF* (27MHz bandwidth) MSK		224–1760$\times$12Kbps (2,048Kbps)**$\times$12

* Satellite
   broadcasting

** including
   sound signals

Introduction of data broadcasting by the Deutsche Bundespost
Klaus Hummel
The Federal Minister of Posts and Telecommunications

The term "data broadcasting" means the distribution of data
information from one source to a large number of sinks. Although
theoretically all physical means could be used as transmission
paths, radio links are generally considered the most suitable
possibility as the cost of radio transmission paths is largely
independent of the number of receiving stations and the places
of destination do no have to be part of an established coverage
system.

Where use is made of frequency bands that have been exclusively
allocated to the broadcasting services it will have to be
carefully examined before the introduction of "data broadcasting"
whether the frequency bands would thus not be put to inappropriate
use.

In compliance with these requirements, the following services
are used or being developed in the Federal Republic of Germany:

1. Distribution services using terrestrial transmitters

1.1 EUROSIGNAL

A telecommunications distribution service was first launched
by the Deutsche Bundespost in 1974, together with France and
Switzerland, in the form of the "radiocommunications to single
or multiple destinations" service called "EUROSIGNAL". This
service has more than 140,000 subscribers at present. It is
expected to reach its technical capacity around 1995 with .....
subscribers.

The area of the Federal Republic of Germany is divided into
three paging zones and that of the Republic of France into

six. In Switzerland, there is only one paging zone.

In each zone, radiopaging centres control the simultaneous
emission of paging signals from the connected VHF base stations.

The information transmitted is optically displayed. Communication
partners have to agree on the meaning of the codes before
starting the service. Figures, letters and speech cannot be
transmitted. German EUROSIGNAL users can also be called in
France or in Switzerland over the public telephone network
via a radiopaging centre of the country concerned.

To preclude any misuse of paging numbers the Deutsche Bundespost
does not publish EUROSIGNAL directories.

1.2 CITYRUF

The Deutsche Bundespost is to launch a new paging service called
"CITYRUF" later this year.

Paging calls will be transmitted in the 450 - 470 MHz frequency
band. The relatively high receiving field strength required
and an effective radiated power of 100 W necessitate a large
number of transmitters, especially in urban areas.

The objective is a 90 % call success rate in the following
conditions:

- in ground floors of buildings,
- for the transmission of 80 alphanumeric characters,
- when the paging receiver is carried on the body, and
- at walking pace.

The service, which will initially be restriced to big cities
and conurbations, will thus provide new features such as the

transmission of alphanumeric messages. This means that callers
using the telephone network can cause small texts or messages
to appear on the display of the called paging receiver.

The following service features are to be provided, for example:

- tone-only: up to four optical and acoustic signals

- numeric characters: up to 15

- alphanumeric characters: up to 80

- single call

- sequential group call

- simultaneous group call

CITYRUF subscribers can be called from the following tele-
communication networks:

- telephone network

- telex network

- teletex network, and

- Bildschirmtext (interactive videotex) network

It will largely depend on the features of the paging receiver
whether the new service will be attractive and accepted
favourably. Due to large-scale integration, modern manufacturing
techniques and the use of integrated antennae, paging receivers
can be as small and handy as cigarette packets. Prices are

expected to be lower than for the existing European radiopaging
service in spite of the high demands on the sensitivity and
immunity to interference of the paging receivers.

2. Satellite distribution service

2.1 The satellite distribution service operated on the basis of the distribution of television broadcasts

·So far, the Deutsche Bundespost has not been able to offer
data distribution services of extensive coverage and operating
at high bit rates other than over wired networks. The existing
HF service "radiocommunications to single or multiple·destina-
tions" was far from meeting the requirements for the desired
bit rates.

Since 1987 the Deutsche Bundespost has been testing a procedure
which uses the teletext lines of a television signal for data
transmissions if teletext is not broadcast together with the
programme. The information is processed in a way similar to
the teletext coding system, inserted into the field blanking
interval of a television signal (teletext lines) and distributed
by satellite together with the TV signal. The 19.2 kbit/s data
stream included ·in the TV signal can be received by private
satellite receiving antenna systems or be carried to the
customers over the Deutsche Bundespost's broadband distribution
network. In both cases a decoder is necessary to evaluate the
data information.

The trial mentioned above should also provide information on
the form a regular satellite distribution service should take.

2.2 New satellite distribution service (VSAT service)

Satellite transmission paths can be made available quickly
and flexibly as required.

In coordination and cooperation with interested customers from trade and industry, a distribution service is currently being tested which is to be introduced officially in early 1989.

The following message services are envisaged:

- receive-only service,

- Data collection service, and

- interactive system.

Using Eutelsat and Intelsat but also national satellite systems (Kopernikus), the service is to cover the following areas:

- service area of the Deutsche Bundespost,

- Europe,

- Atlantic area, and

- Indian Ocean area.

Depending on the requirements, dish antennae with a diameter of 60, 75, 90 or 120 cm will be used. The interactive system requires antennae with a diameter of 1.2 to 1.8 m.

Transmission bit rates can be provided for data streams of 4.8, 9.6 and 19.2 kbit/s, with error bit rates of 10^{-5}, 10^{-6} and 10^{-7} respectively.

The new distribution service should be available 24 hours a day at 99 %.

The service also allows the establishment of closed user groups.

3. Information for multiple destinations transmitted in the form of data in connection with broadcasts

Data information is transmitted together with broadcast signals, particularly with VHF and television signals. The data transmitted should exclusively contain information associated with the programme. For the sake of completeness, however, I should like to mention and briefly describe this system called "Data Broadcasting".

3.1 Television

3.1.1 Teletext

Teletext is a system providing viewers with information associated with the programme or of general interest, which is transmitted in the form of data within the television signal.

3.1.2 VPS

VPS is a technical system used to synchronise the start and stop of videorecording to the beginning and end of a programme.

3.1.3 VPV

VPV (teletext programmes videorecorders) is a new technique which uses the programme information on teletext pages for the easier programming of videorecorders.

3.1.4 TOP

TOP (Table of Page) is a technique making it easy for users to call up pages in the teletext system.

3.2 Sound broadcasting, RDS

RDS (Radio Data System) provides radio listeners with information (name of radio station, traffic reports (ARI)) transmitted in the form of data in the FM radio band.

However, it is currently being examined whether this system would also allow the transmission of services similar to "Cityruf". The high availability of VHF transmitters which can be received everywhere due to their great field strength could make such a service highly attractive.

4. Conclusion

The fast technological development will make the transmission of information by "data broadcasting" more and more important. The new MAC standards for transmissions offer particularly favourable opportunities.

However, the development of new services in this field will ultimately be determined by the market requirements. The Deutsche Bundespost will use any technique available in line with demand.

- To make a single call, the caller addresses the paging receiver
  by means of the paging number.

- A special sequential group call number is used to address
  several receivers together. These receivers are normally
  called by means of their individual number.

- The service features are comparable to those of EUROSIGNAL.
  All the receivers have the same code number. They are called
  simultaneously by one call using a common group call number.

RECENT PROGRESS IN OPTICAL CARDS

Nagahiro Gocho
Olympus Optical Co., Ltd.
2-3 Kuboyama-cho, Hachioji-shi, Tokyo, 192 JAPAN

INTRODUCTION

For thousands of years, paper has been the main medium for recording, archiving, transporting, and displaying data. The merit of paper is that no peripheral devices are needed to review the information. But recently, the volume and demand for information handling has been increasing rapidly and paper has begun to show its demerits as it is bulky and heavy in large quantities, mailing costs are high, random access is difficult, and the information is easily copied. To combat these difficulties, one solution was proposed in the early 1980's. That solution was the Optical Card.

Because writing on the optical card is performed by a laser, a large amount of information can be stored in a tiny area. This results in a number of benefits, a few of which are:
(1) Large Capacity: 1 - 2.5 MB per card (1000 pages of A4 text)
(2) Low bit cost/card cost: 3 KB/Pfenning, 8 Marks/Card
(3) Portability: Credit card size
(4) Safety: Pre-recorded or Write once, Encryption possible
(5) Durability: Unaffected by magnetic fields/static electricity

This paper will present a brief outline of the current status of the Optical Card and Optical Card Reader/Writer systems and examine some of the doors opening to this new industry.

OPTICAL CARD READER

The Optical Card Reader (OCR) is a read-only model used for retrieving and manipulating information from pre-written ROM cards. The Olympus OCR combines a display and keyboard in a portable model for the following features:

1) Information retrieval and data calculations are performed by a built-in CPU.
2) Data input is possible using the integrated keyboard.
3) A large LCD display is used to view information and interactions.
4) The exchangeable ROM cards provide the data information and necessary interaction programs.
5) Peripheral device connection (computers, printers, monitors, electronic musical instruments, etc.) is possible through an integrated interface.

OPTICAL CARD READER SPECIFICATIONS

Reading Speed: 100 Kbits/sec
Error Rate: 10^{-9} to 10^{-12}
Input/Output: Built in keyboard and LCD display
Card Insert/Eject System: Automatic (Eject by Eject Button)
Applicable Card: ROM Optical Card (54.1 x 85.7 x 0.76 mm)
                 0.5 MB to 2 MB Capacity
Operation Modes: Stand Alone/Peripheral Device
Interfaces: RS232C or Centronics
Dimensions: 290(w) x 69(h) x 223(d) (mm)

OPTICAL CARD READER APPLICATIONS

The ROM card is well suited for distribution of the same
information to a large quantity of users. Many applications are
possible when this card is combined with the Optical Card Reader's
input and display, data searching, and calculation capabilities:
* Publications Index   * Manuals
* Telephone/Address Directory   * Inventory Lists
* Electronic Music Memory   * Parts Lists
* Time Tables (Airline/Railway/Bus)
* Insurance Rate Table (and calculations)

The optical card is more advantageous than paper as it is easy to
carry or mail large quantities of information, the bit cost is
low, and information protection is possible by data encryption.

OPTICAL CARD READER/WRITER

The Optical Card Reader/Writer (OCRW) is a compact Write Once Read
Many (WORM) optical system. It contains a controller and power
source which allow personal computer connection with a single
cable. An integrated automatic card cleaner and uniquely designed
error correction circuitry reduce the error rate to less than 10^{-12}.
Various types of interfaces allow direct connection to many
systems. Application software is easily developed using a device
driver designed for the optical card.

OPTICAL CARD READER/WRITER SPECIFICATIONS

Card Size: 54.0 x 85.7 x 0.76 (mm)
Media Size: 35 x 85 (mm)
Storage Capacity: 1 to 2.5 MB (per card)
Access Time: Less than 1 sec.
Reading Speed: 64 to 128 Kbits/sec
Writing Speed: 16 to 32 Kbits/sec
Error Rate: Less than 10^{-12}
Card Insert/Eject: Automatic (Eject by Eject Button)
Card Cleaning: Automatic
Interfaces: RS232C, Parallel I/F, SCSI, others
Dimensions: 232(w) x 140(h) x 265(d) (mm)

OPTICAL CARD READER/WRITER APPLICATIONS

Because the card is write-once, the risk of accidental erasure or media destruction by magnetic fields or static electricity is non-existent. The flexibility and compact size of the card allows standard mailing and permits storage in a wallet or purse. Illegal alteration of media is nearly impossible, and the low cost makes erasing and rewriting on the same card unnecessary.

Thus, the WORM card is well suited for updatable information which must be carried or mailed. Current possibilities include:
* Medical Card
* Factory Automation Card (CAD/CAM)
* Financial Passbook/Transaction Record
* ID Card
* Maintenance/Repair Records
* Confidential Information
* Software Distribution/Updating

EXPERIMENTAL/FIELD TESTS

Some field tests have been completed, others are continuing, while still more are planned in Japan, Europe, and the U.S. Most of the tests are in the medical field, while others are in the financial, ID card, maintenance, and electronic publishing fields.

(1) Medical Field
The Medical Optical Card contains basic personal information (i.e. name and address) as well as a medical history including weight, height, blood pressure, blood chemical tests, electrocardiograms, pharmaceutical prescriptions, etc. Doctors can easily access the data, which is shown as a graph on the computer monitor, to study the tendency of each item. This provides a great help to diagnosis. Medical Optical Card field trials have been performed in Japan at Ohmiya Hospital, Tokai University, Natmec Nanasato Hospital, Hakushu Town, and in the U.S. at Baylor College. Further Medical Card field trials are planned in Japan, the U.S. and Europe.

(2) Financial Field
Financial Optical Cards are used for transaction records and personal information. Sumitomo bank, Olympus, and Omron used optical cards as a prepaid card in Sumitomo bank's cafeteria beginning in June 1986. The test provided Olympus with information useful for improvements in the machine, which have already been implemented.

(3) Other Fields
Several trials are planned in various fields in Japan, Europe, and the U.S. These will be announced in the near future.

STANDARDIZATION

Standardization activities were accelerated in 1988 in Japan, Europe, and the U.S. In Japan, the ISO/IEC JTC1/sc17 adhoc Optical Card Committee (sponsored by the Japan Business Machine Makers Association) began discussions in August of 1986 and published a draft of a standard for parts 1, 2, and 3 (JBMS-39-1988) in March of 1988. Part 4 is currently under discussion and will be published in the near future. In Europe, the Drexler European Licensees Association (DELA) began discussions on standards in 1987. DELA is holding monthly meetings and is scheduled to complete a first generation standard by the end of 1988. In the U.S., ANSI X3B10.4 Optical Memory Card meetings are held several times per year. The most recent meeting was held in Washington D.C. in early September 1988, where a draft (parts 1 to 4) was submitted.

SUMMARY

The low cost, high capacity, portability, and high security of the optical card qualifies it for a wide variety of applications in the fields of medical history records, financial information records, maintenance/repair information, publishing, education, personal identification, and confidential information exchange. The Optical Card Systems have progressed to the field test phase. More activity will occur next year, with larger scale implementation beginning in the early 1990's. With continued effort and support, optical card systems will have the capability of meeting with worldwide success.

REFERENCE

N. Gocho, "The Optical Card System: Description and Applications", Optical Information Systems '87 Conference proceedings, P140-144, Dec. 1987 (New York, U.S.).

CHIP CARD FUNCTIONALITY AND APPLICATIONS

Klaus D. Wolfenstetter

Research Institute of the Deutsche Bundespost

ABSTRACT

The rapid growth of communication services and informa-
tion processing and their increasing mutual influence
involves also new challenges for the global and open sy-
stem concepts and related technologies. With the
multifunctionality of technical devices, worldwide stan-
dards and recommendations, neutral interfaces being
independent of the producers, data protection and
security features etc. only some of these ambitious aims
are mentioned. Therefore, according to the design and
conception of future modern information and communication
systems, chipcard technology will play an important role.
It will emerge as a service medium of the future and will
extend to a variety of new applications and problem
solutions.

The reasons for this development are manifold:

The (conventional) credit card size microcomputer card
is the ideal medium for anyone to provide future
communication and information processing services with a
maximum of comfort, multifunctionality and security.

These requirements essentially are based on the
"intelligence" and high memory density of the chips, whose
extraordinary properties are

- high memory capacity

- high computing power

- high reliability

- high security against manipulation

- low cost card reader device

- standardized interfaces or transmission protocols
  between chip and reader.

The technical medium chip card enables services in numerous of professional and private life areas such as

- cashless buying via
  - home banking and teleshopping (e.g. electronic purse)
  - EFTPOS

- coinless telephone calls via public telephones or radio telephone systems

- collecting, storing and processing of information e.g. according to
  - medical data
  - ID card data
  - transaction data etc.

- controlling or steering processes or computer programs

In essence most of these services have common security requirements such as

- access control to computers or network switching centers

- access legitimation to data bases

- confidential exchange of messages

In order to realize all of these tasks the following security services have to be provided for the active system parts:

- protected storage of data in the card

- identification of the subscriber with respect to the card

- mutual authentication between card and system (resp. terminal)

- mutual authentication of communication data via digital signature.

- data encryption in the card.

The paper intends to outline some of these security applications. Beyond that we try to describe the various technological and conceptional demands arising from the security problem.

The Present Situation of CD-ROM in Japan

   The first case of the practical use of CD-ROM in Japan was a

dictionary of techno-scientific terminology (Sanshusha) published in

1984. The ability of the large memory capacity in CD-ROM was fully

utilized in this case. Moreover, publishers have attemped to use

CD-ROM in the publication of prestigious existing dictionaries,

including the Kojien dictionary (Iwanami Shoten), and are expanding

the range of CD-ROM application by combining it with word processor

function. Various data bases are under CD-ROM programming, too.

Information publications on books, magazines and patents are also

becoming widespread as package-type products.

   Under these circumstances, publishing houses having a strong

interest in electronic publishing gathered and inaugurated JEPA (the

Japan Electronic Publishing Association) in September 1986. At present

the association includes not only publishers but also electric

appliances makers, computer makers, printing firms, software firms,

chemicals makers, book publishers, record companies and the like from

various industries, and participants are widening exchanges among

themselves. To promote new media like this, user needs must be

effectively communicated to makers, and JEPA's formation proves the

increasing awareness of this. The menbership of JEPA exceeded 150 as

of October 1988 and more firms are expected to participate from various

industries. One of key subjects of study at JEPA is standardization.

It is felt that without standardization, this business cannot exist.

This was learned from the history of major media. ISO 9660 became a

global standard for CD-ROM, and efforts are continuing to generalize

this format by adding conditions that will enable the use of the format

not only in Japanese-language area but also in the whole kanji-letter

area.

The Future of Electronic Publishing

The expression "new media" was much in vogue several years ago, but despite its popularity and great expectations in industrical circles, its successful cases were very few. Therefore, a cautious attitude is still prevailing toward the term "electronic publishing."

However, the above-mentioned improvement in data bases and practical use of package-type media (CD-ROM, etc.), less expensive than on-line systems, have been reducing retrieval cost and making devices very easy to handle, thus creating strong hopes for their future dissemination. Nevertheless, the use of on-line system media in parallel is indispensable to accessing up-to-date information. For the present, main users will be limited to business enterprises and researchers, and the popularization of these media among individuals (homes) will remain yesrs away. Progress in input, editing and DB (data base) programming technologies on the part of IPs (informatoion providers) has been very

conspicuous, while the diffusion of personal computers among users is

increasing. Considering this, it can be safely said that the environment

of electronic publishing is steadily improving. But, the arrival of the

time for its individual use will depend on when handy and highly

interactive equipment. such as CD-I, (First "The Visual guide to plants"

prototype was introduced in Oct. 1986 by Shingakusha and Hitachi.) will

become available at low cost. And even if such a time arrives. people

will still choose to read literature in the existing printed from.

Michio Horiuchi

Video Communication in the Business Field

Volker Steiner
Federal Ministry of Posts and Telecommunications

Abstract

High Quality Videocommunication in the commercial applications is an important strategic element in introduction of broadband communication.

The first major application pilot - Videoconference - has created valuable experience in the fields of network, terminal equipment, service offerings and customer-market-reaction. On this basis the actual concept of development videocommunication market by the following aspects:

o   Network aspects

The national broadband forerunner network (VBN) will be implemented by the end of this year, with full automatic self dialling capability. Digital picture distribution via satellite, integrated by gateways into the VBN and the terrestrial TV-distribution network will be implemented, as well as adaption to different coding standards.

o   Terminal systems

The early development of videocommunication workstations, multifunctional/multimedia terminals and broadband inhouse systems is a main objective to be carried out by the BERKOM-Project and other pilots.

o   Application/service development

Application pilots in the fields of Telemedicine, Telepublishing, distributed factories also in the framework of the BERKOM-Project, the RACE and AIM-programmes of the European Community will foster market exploitation and service definition.

o   Research/Systemdevelopment

New Codec-generations [e.g. 34 Mbit/s, m x 384 kbit/s (m = 1 ... 5), n x 64 kbit/s (n = 1,2), p x 64 kbit/s (p = 1 ... 30), HDTV-Codecs] and terminaltechnologies including user-friendly man-machine-interfaces are main areas of necessary activities.

Further steps for integration of interactive and distribution video communication services and extension of those services offerings into the private area are intended but depend on the results of the activities explained.

付録3　コンピュータ分科会アブストラクト

付録 3. コンピュータ分科会アブストラクト

Overview of TRON Project
(TRON Project Impact upon the Computer Culture)

Norihiko Ito
Department Manager,Microcomputer System Department
Hitachi Ltd.,Musashi Works,
1-20-5chome Johsuihonchoh,Kodaira City,Tokyo,Japan
TEL 0423-25-1111,FAX 0423-26-2154

1. Preface

Nowadays TRON Project has absorbed considerable public attention. A lot of journalists also are greatly concerned about it, so we often read their accounts, but they always do not introduce the exact intention of this project's participants. In spite that they don't know much about what TRON Project is, this may be one of human being's bad habits, some critics have discussed and confused the general public by their wrong information.

Making TRON Project's intention as clear as possible, I am reporting TRON's coming movement and impact which may be given to the computer industry.

2. The Driving Forces of TRON (The Realtime Opesrating System Nucleus) Project

Basesd upon the idea of Dr. Ken Sakamura, Assistant Professor of Communication Science Department, the Faculty of Science of Tokyo University, TRON Project is giving strong influences and impacts to today's rapidly developing computer culture. The purpose of TRON Project is to create the total computer culture including home, office and industrial environment control systems. In order to be able to correspond to a lot of occasions, TRON Project has some sub-projects and also a consistent thought that computer should not be for some specialists, but should be:

(1) easy to use for everyone.

(2) well designed for human being.

In the computer industry today it is said to be a kind of common sense that a new computer system has to be designed careful enough so as to have software compatibility with the past conventional products. Even if a computer could have capital functions, most of people believe such computers are never used if they do not have software compatibility with the past products at all. (Lots of people still think this way.)

In order to create really new and independent computer culture, we have to originate the new architecture and the development environment including OS and languages then to make application software and hardware from the very beginning. These works need huge time, labor and money. After all no one has

ever tried this expensive risk yet.

A lot of manufacturers have produced only makeshift wordprocessors and personal computers by combining software and hardware products which are currently available. As it is, they have become convenient ones. I am, however, in doubt whether they are really useful for everyone. Therefore it is proposed to choose completely different approach in the TRON Project as follows. First of all, we create easy to use Man-Machine Interface. Then we plan what equipment or OS specification should be. Finally we study and create the computer architecture in which users can make the best use of OS specification thereof. Dr. Sakamura's idea, to create the total computer culture for mankind with appling the latest technology available in the 1990's, catches engineers' hearts, interests users and influences even some big businesses. The power seems like a burst of an oppressed volcano. The growth of today's TRON Project looks like such an eruption.

TRON Project has some driving forces.
First, it is the ambitious but simple motive to make something you have never seen before. It would be almost impossible for just one manufacturer to create the total computer culture in its way. Every manufacturer's technology range may be smaller than what TRON Project requires. For example, a well-known LSI manufacturer may not always have a good experience in making a personal computer, or a company who is well experienced with making a personal computer cannot be a good intelligent house builder.
Thus, Dr. Ken Sakamura is strongly supported by the member companies of TRON Association with having each company's knowhow and latest technology skill in each individual industrial market segment. That is, TRON Project's reserch activity is supported by wide variety of each company's industrial experience, and it is very grateful each other to have such an unintentional systematic cooperation that happened in TRON Project. As such, we can say that it is a very specific point of TRON Project to create a new computer community with having many companies' cooperations. The very simple and ambitious idea to create something new that you have never seen before and something really good for mankind does not likey fit Japanese company operation policy, but current TRON Project activity is said to have already completely overcome such a micro level obstacles. It is not too much to say that we are trying to create new markets with TRON Concept.

Second, we have to recognize the fact that most Japanese workers understanding as to problems of trade friction, copyright and intellectual

property ownership has been remarkably changed. If we use other manufacturers'
or people's ideas, we can easily guess we may come under suspicion of
plagiarism. Therefore, we can say that it may be a very challangeable target
but most important point that we try to create the original computer culture
and to contribute to people and countries all over the world. In general,
almost all of the properietary computer architectures were designed by limitted
number of engineering people in each private company who have been trying to
protect them as its intellectual property for years. Therefore, it may be
subject to argument if these properietary computer archiecture may be freely
used by any other companies. However, the new computer architecture which is
going to be defined in TRON Project will be established as one of the world
wide usable standard and will be put into public domain for anybody for free of
charge to use. We have never heard such idea and philosophy before so that
most of people say it is really a revolutional activity.

Third, TRON Project is greatly supported by many users who wish to use a
personal computer which is really well designed for human being. We can say
that the most of computer users are forced to use a computer which is designed
by computer manufacturers under manufacturers' view point. Actually it happened
that those people who can use a wordprocessor manufactured by A company cannot
use the other one by B company at all. Users have been embarrassed by also
different file formats by every manufacturer, and yet each manufacturer has been
promoting hard that its own product is best. Therefore users feel embarrassed
when they want to buy one.
    Since every manufacturer is in severe competition to produce own personal
computer and/or word processor before establishing a common industrial computer
standard, it looks very difficult to stop such an industrial stream. However,
people in TRON Project recognize such a fact is a very big problem. Therefore,
those people are tring to promote TRON Project so that as many users as
possible may recognize the existence of such a problem and may know accurately
what the TRON Concept is with having adequate support by all kinds of mass media.
Some day in near future, we believe the office automation market place will far
greatly grow up and we don't have to feel any confusion in choosing a computer,
if we can produce such computers as having complete media compatibility,file
compatibility,program compatibility,and man-machine interface compatibility
among those computer manufacturers.

    There are a lot of other driving forces which can not be written in detail
within limitted space. But TRON Project is the project which fittingly meets
the needs of the times.

TRON Project consists of some sub-projects which need all-round technologies.Any manufacturer that may have an interest in TRON Project should actually take part in any of the sub-projects. Only watching the project may not be meaningful,but it is very important to participate the TRON Project and study with us.   At the end of the 1990's, TRON Project must be appreciated as a most significant project in the technological history of the world. Toward creating useful computers for mankind, we have been and will be bending our efforts continuously.

3. May We Rely on Common Sence in the Industry?

All kinds of business have their own common sense, and it is often said that the novel management without having a common sense usually brings to bankruptcy. On the other hand, people on the opposite side also fail at the end when they never believe temporary practical expedients. We know, moreover, quite large number of cases to change a foolish idea into today's common sense. These show us the neccessity that we sometimes have to change our way of thinking according to the technology progress or change of circumstances and times. The first manufacurer that has appreciated these changes can get an advantage over the others.

When a floppy disc was introduced in 1975, disc engineers were very surprised and confused at its eccentric concept:

(1) It does not have a pivot but only a round hole.

(2) It is in contact with the magnetic head.

(3) In a paper envelope, it always rubs with it.

Most of disc engineers regarded it as a ridiculous product, and did not believe that it could be used as a reliable file media. But half a year later everyone recognized that those day's absurd product was the beginning of today's OA society.

In case of a watch, we can easily see the technology progress. Because we often see them selling in a bowl and find many at home given as a premium. For example, a girl was given a wrist watch as a premium when she bought a junior high school uniform and her grandmother said that it had been so extravigant and ridiculous to give a wrist watch thanks to buy nothing but a school uniform.

Some years ago, it was the symbol of rich and more expensive than anything including any clothing. However, they have become cheaper by mass production and a premium of clothes on the contrary. We can no more say a wrist wach is a simbol of luxury unless it is decorated with gold or jewel.The common sense of watches has been changed remarkably.

In case of a camera, cirtain level of expert knowledge was required to handle a camera some years ago. But today we don't have to have any special

technique and/or expert knowledge in handling a camera. We have only to press the shutter for a subject and then the camera itself brings the subject into focus, winds the used film and even flashes a lamp if necessary. Because of such automatic camera introduction the demand of camera has been greatly expanded and those like the aged or kids who have never used a camera before have come to use an automatic camera very easily. On the other hand, for those who have professional knowledge, the manufacturers produce cameras designed for professional use. From the beginners to the specialists, camera manufacturers produce all kinds of cameras.

How has personal computer business been changing?

It is the fact that a personal computer is useful, but we are vexed at it. For instance, there is no software compatibility among PC's even using the same OS in the same CPU, if the PC manufacturer is different. It can be said also for files and printers. Even how to use is all different, so we have to read each bulky manual for each computer. In spite of these simple facts, some people say against TRON Project trying to solve these problems, "There is no succeeding, because they have no compatibilty with past products." Althogh they never know the real philosophy of TRON Project, they sometimes pretend they know it well.

The reason why TRON Project has recently been getting supported greatly is simply coming from users' consciousness. In other words, there are many people who desire to use PC which is really well designed for human being as we experienced with the camera industry. Nevertheless, there are still a lot of PC manufacturers who might be poor at recognizing such users' desires or their attitudes.

Everyone is likely to think of his or her future as the extension of the past. At that time the more we have strong past experiences, the more we make our future narrow. In proportion to our ages, we come to stick to our ways of thinking and not to accept new concept easily. But we have nothing eternal, so we always have to have changed our ways of thinking. It may often be said nothing can hold its shape forever also in the industry. Any personal computer can not keep the same style forever having compatibility always with past products. Most of people believe that MS-DOS, which is an OS incorporated in more than 90 percent of today's personal computer, must be continuously used also in future. This is, however, a simple future image that people who are engaged in PC business are likely to describe. Personal computer may not be used widely spread to people who have never used a personal computer if we could not solve those problems described as above. Even from a PC business point of view, I am absolutely discontented with the PC under present conditions. It is

now coming when we should consider the direction where the personal computer is going.

People who are doing business in today's personal computer industry are likely to believe that MS-DOS will never change it's No.1 position at least for coming 10 years and did not pay much attention to Macintosh at it's debut, which is becoming a considerably strong competitor against IBM-PC. Looking at the fact that only ten years ago MS-DOS never came into existence, nobody can say the second or the third MS-DOS like historical new OS debut never takes place within next ten years. At present more than half of workers developing microprocessor apllication system use or try to use C language, but there were very few who used it ten years ago.

Before we persist in the common sense, we should put it flexibly into the common sense that no one in our computer industry can exactly know what happens in future.

Some people are saying, "BTRON specification key board bothers us, because it is out of the standard." To oppose it in Dr. Ken Sakamura's term, they are the same as those who cannot stop smoking offer the cigarettes to others in spite of knowing hazard to health. In short, we don't care when they use their fovorite and accustomed computers, but they must not advise others in particular young people to use them." I quite agree with him.

At first when we brought an engineering workstation into our office room, some engineers complained of it. For example, "We have no time to learn how to use," or "It takes more time than the handwriting," or "It is not compatible with the way we used to do." Human being might part into two types, those who have a spirit of enterprise and the others who cannot easily accept new concepts and environments. Anyone, indeed, may not be apt to change his or her way if not necessary. I think, however, that these people who would persist in their ways are not eligible for discussing the future coming computer culture.

Through TRON Project activity I recognize that people likely fail to be objective. We have our own subjective thoughts. But we have to settle the standard as soon as possible before computers are going to be used more greatly. The later we settle the effective standard, the bigger our social loss will grow.

4. The significance of TRON Project
(1) The Teamwork between All Types of Industries

You do not always see only one industry in TRON Project. Companies who are joining into TRON Project are from all fields of industries--semiconductors, computers, office automations, printings, buildings, air lines, music

instruments, power electricities, automobiles, universities and so on. Each company and/or the users are eager for TRON Project's success from each point of view.

So far we know some facts that few types of industries have assembled together to settle a standard or to establish their joint venture. But we have never seen that such many types of industries had discussed to settle only one standard before TRON Project.

It often happens that too many people discussion results in no output. In case of TRON Project, however, Dr. ken Sakamura is so goodat leading them that each sub-project can have the definite specifications as a whole.

MTRON Design must be one of the reasons why many types of industries take part in this project. MTRON Design which Dr. Ken Sakamura proposes is to use and combine a great number of computers as tools to help human being thinking and action. A lot of types of industries concentrate their attentions on the possibility whereby MTRON Design widely expands the computer application field and creates various new markets.

(2) The Rapid Rising of The Valuation for TRON Project

People in general have come to appreciate TRON Project highly. If you examine their consciousness, you will know that about 20 percent of Japanese people at the beginning of 1988 already believe TRON Project's future success. We don't have to be disappointed the result that only one fifth of people believe it, because all of them who answered to the questionnaire do not correctly know the intention of TRON Project. Considering this fact, the number of 20 percent is not the low percentage. The more we are going to send off TRON Project's products to the market, the bigger number of people will come to know the exact TRON Project philosophy. Then it is not said long before rising up to 30 or 40%. We have to recognize that the percentage are rapidly changing.

(3) The Fair Profits for All the Companies

If only one company profits and all others lose in the same project, the project becomes out of balance, cannot be promoted any longer and then comes to fail at the end; besides, this is also an obstacle if one company doesn't allow others to use its intellectual property and/or a patent which might be incorporated into external specification of TRON concept product. All of the companies, taking parts in the project, need to have the fair profits according to their labors. TRON Project never has these problems, for all participants have taken the attitude to co-operate with each other for creating the total computer culture. As the result, the spirit of the fair profits for all the

companies comes into existence.

(4) TRON Project for People all over the World

"Personal computer should not have only English but all languages for all
people and also for those who cannot speak English," Dr. Ken Sakamura has been
saying.   Though TRON Project was born in Japan, we are not going to make
computers for only Japanese. We, moreover, have never intended it for Japan to
have the advantage of computer industry. We do think that a PC should be used
as a tool which assists the thinking for all people in the world.

Dr. Ken Sakamura strongly proposes that a personal computer should treat
multiple languages. Korean hungle, Chinese kanji, Thai character, Arabic
letter, etc.,for example, cannot be expressed within only 26 alphabetic
character set. As you know, eight-bit code computers are not enough to accept
these languages. A personal computer cannot be used without having any relation
with each country language culture. We believe TRON Project in Japan will be
able to contribute to the technology progress in the computer industry all over
the world including Asian countries.

(5) The Esteem of The Intellectual Property

It is most important now for Japan to create Japanese own product concept
towards all over the world. Some people in foreign countries say that the
Japanese are apparently far ahead of in making substantial improvements on
existing technologies from the United States and Europe, and incorporating
these advances into highly marketable products. It is worthy to make
improvements on existing technologies and/or product, but it is worthier to
create own product concept than making any improvement. In order not to arouse
those suspicions any longer, now Japanses have to try to produce Japanese own
product concept. Dr. Ken Sakamura also says, " Japanese is lacking in this
recognition."

(6) Marketing is the Subject of Each Manufacturer

TRON Project is not the place to market the developed products, but each
participant only to support Dr. Ken Sakamura's research activity.   TRON Project
is the place where each participant co-operates to establish the new computer
industry standard. Therefore the marketing is the subject of each manufacturer.

(7) Educational Personal Computer in Japan Based upon BTRON Specification

With the satisfacion of some essential conditions, CEC(Center for
Educational Computer) has regarded BTRON specification as the OS for Japanese

educational personal computer. This may give strong affection to Japanese future computer market place. Though it may be frequently discussed until CEC ultimately settles the specification, BTRON specification is more hopeful and effective than any other ones in the educational field. But some journalists critically write that CEC specification does not emply BTRON key board and that no one use such OS with full of bugs. We take it for granted that trial products might have many bugs. In spite of the fact that the bugs have nothing to be connected with TRON Philosophy, they say that BTRON Concept is in despair because of bugs. Such articles may be able to pull our progress back out of the promotion, but they are too absurd and meaningless to get themselves in honor. It is lately that CEC started to discuss the specification. Before long the bugs will be fixed as time goes on. We are going to carefully watch the direction of this discussion.

(8) The Engineers Enthusiasm with the First Attempt in the World

There are many cases that a lot of Japanese people don't appreciate the first attempt in the world at its early stage of research, and they always insist of the safe and steady management above all. It often happens that they recognize how important it has been after other nations' comprehension.

As you know, Japanese companies are apt to persist in their conservative managements. In plain words, they sometimes invest big amount of money in order to catch up with other leading companies, but it may be often the case that the original plan or idea which no other firms have ever tried before likely faces difficulty in getting the investment from the management. TRON Project is such a new and original plan with the greatest expense, so that they may well think cautiously whether they take part in it or not. We must, however, think of the fact that best sold products have often been developed by the engineers' eagerness and enthusiasm. TRON Project is the place whereby we can grow people's enthusiasm which may give big extended influence and impact to each company. We would like to share such experience with each other. The most important and significant thing is to develop products in TRON Project. In addition, it has another meaning to give engineers the precious and lively experience to challenge the first attempt with having other companies'co-operation.

(9) The Strongest Developing Power in the World

It is said that the engineering power developing 32 bit microprocessors based upon TRON specification is stronger than any other 32 bit micro's. Above all, manufacturers taking part of in Gmicro family have their own development of each 32 bit microprocessor so that entire investment for Gmicro family

including its peripherals is going to be huge amount and that users would have a biggest opportunity to obtain system LSI's one after another as a result. According to TRON Project's spirit, even manufacturers other than Gmicro family may have a lot of opportunities for making use of the external specification. This is one of TRON Project's noteworthy points.

(10) The Different View Points for Future Computer Popularization

Some say that computers and those softwares have spread already so that it is too late to settle the computer standard from now on. The others say that they have just started spreading but we have still enough time to settle the standard before the rapid diffusion. The judgements are quite different.

The progressing speed of hardware seems far faster than that of software at present. We can say that because of the speed limitation of the software progressing the hardware development itself is very badly affected in many cases. If we continue to develop a new product within the framework of software progressing, such developments may not come to meet the needs of the time. When people come to know that the existing software cannot satisfy the hardware progressing because of its slow development, they cannot help deserting the obsolete software. For example, we wouldn't use the software which expresses only alphabets and katakana(Japanese plain letters) on the personal computer which can deal with even figures and kanji(Japanese complicated letters). Most of the past products have their histories like this. In short, they were deserted because they couldn't meet users' requirements. It would be the semiconductor industry that has been controling the developments of both hardware and software. The semiconductor industry may hit the dead end of technology progressing in far future, but it will keep leading and controling the computer industry until then.

5. The Misunderstandings against TRON Project

TRON Project has been rapidly known to people within these few years. Project informations have been brought by many articles on newspapers and/or magazines, however, there are quite a few articles which report random and inaccurate informations about TRON Project, and then people understand TRON Project incorrectly as a result. In particular, there have been some cases where people who are not concerned about the computer industry have sometimes criticized TRON Project without having actual knowledge of it. I do not mean that TRON Project has no defects. If their strict criticism were based on the fact, then I don't mind but appreciate and listen to them with all my heart. I would like all people including them to dicsuss TRON Philosohpy with having correct knowledge. The followings are some of examples of typical misunderstandings.

(1) TRON Project has no copyright protection policy?

According to Dr. Ken Sakamura's concept, everyone can freely use the specifications and/or the standard which are defined in TRON Project, however, it does not mean that there is no copyright protection for those documents which describe the TRON concept, specifications and/or standards. The people or companies that have developed OS and/or LSI based on TRON specifications have their own copyrights, and they may not distribute the developed OS with free of charge. When the development being completed and the specifications being clearly defined, only those external informations and/or specifications will be put into public domain by TRON Association. Those informations such as implementation data, maskworks, firmwares, microcodes, software source codes,etc. are of each companies' intellectual property which should be legally and properly protected.If there may be any company who wants to develop those specifications with us, you should become a member of TRON Association and take part in any technology committee of it. We are quite willing to welcome and to work with those people who want to discuss new computer standard in our technology committee, who sympathize with TRON Concept and who positively want to challenge this project.

(2) There is no practical product image in TRON Project?

There are some people who say, "Dr. Ken Sakamura's books which are written about TRON Project show some kind of dream and do not describe any practical product image, therefore, he seems to be untrustworthy." All practical development and sales depend upon manufacturers. So Dr. Ken Sakamura might think it discourteous and impolite for him to write about the practical products before manufacturers announce their developments. Before long each

manufacturer will publish books, pamphlets,and/or catalogs which may describe detailed specifications of products. If you want to know the practical product image, you should read them. Also all kinds of standards will be published by TRON Association as soon as those specifications are clearly defined.

(3) TRON Project is a kind of insurance policy for each company?

At first, there may be many companies who have decided to join in TRON Association only for the purpose of watching the outlook and getting technical informations. This project, however, would have never been promoted at all if all companies only kept watching.

Companies, who are seriously supporting Dr. Sakamura's research and promoting TRON Project, have never thought of TRON Project as a kind of insurance policy. Someone might misunderstand TRON Project in this regard, because companies wouldn't speak about their developing products before completing the development. We never regard TRON Project as an insurance; besidesd, you will come to know the practical product image when we complete the developments and begin to speak about them. In fact, it is strategically much better for introducing philosophy first and then introducing produts next to the market place.

(4) TRON Project is only for Japanese to advantage over others ?

TRON Project was certainly born in Japan, but the purpose of the project is not to have the advantage over other countries. TRON Project is to have very wide and generic purpose to create the total computer culture to help human being easily communicating with others all over the world. Thus we are annoyed by saying that TRON Project is only for Japan. Reading such an incorrect article which might be written by the journalists' prejudice, other journalists might have accumulated their own TRON knowledge and then as a result those journalists say "TRON Project promoters have so strongly insisted to produce MPU and/or OS only for Japanese that TRON Project will be totally isolated in the world." None of TRON Project promoters have ever thought that TRON Project is only for Japanese. TRON Project is perfectly open to anybody in the world.

TRON Association was under the control of Japan Electronic Industry Development Association (JEIDA) until March 1988, but on April 1988 we established a corporation aggregate called TRON Association for the purpose of being independent from JEIDA, because JEIDA was established by Japanese Government aiming Japanese electronic industry development and therefore is not adequate to promote TRON philosophy which challenges to make international standard.

(5) We can compare TRON Philosophy with MS-DOS or UNIX ?

   We sometimes read articles that TRON is compared with MS-DOS or UNIX. The
articles, however, are meaningless because TRON Philosophy is quite different
from MS-DOS and/or UNIX. While MS-DOS and/or UNIX are only an "operating system"
, TRON is philosophy intending to create the total computer culture including
man-machine interface, standardization of removable parts for PC, communication
protocol, microprocessor archetecture, operaring system archetecture and so.
If you insist on the comparison, you will know that you have to compare UNIX or
MS-DOS with only the kernel of BTRON specification operating system. BTRON
specification contains, for example, difinition of keyboard layout, a smart pen,
man-machine interface, etc. which are not defined in UNIX or MS-DOS.

(6) Ideas at an university are of little practical use ?

   This is quite an impolite opinion for people working in universities. Some
self-conceited ideas might sometimes have practical difficulties indeed. TRON
Project, however, is very much well supported by a number of companies coming
from various area of industries so that it is never self-conceited. Since TRON
Association is an aggregate of corporations, we sometimes face difficulties to
harmonize different opinions. Dr.Ken Skamura, however, controls TRON Project
very well and his leadership attracts the participants after all.

(7) TRON Concept does not have new concept ?

   There are some inadequate opinions saying that TRON Concept consists of
combinations of all of those techniques and ways of thinking we have had
already so that there is nothing new.

   In TRON Project, Dr. Sakamura and the participating companies don't make
clear the process at every step to outsiders, and we are going to clearly
announce all of those technical data, namely, standard specifications after
difinition being completed. We, therefore, agree there might be some cases
unclear to outsiders till we open the specification.

   We do not always deny the conventional way of thinking. We often employ
conventional ways and we develop new concepts when we really need them.
Important thing is to organize those various technologies into systematic and
practical total concept with incorporating new ideas.

   In general, anyone who only criticizes others without doing any action is
not welcomed. Now it is the time to try TRON Project actually.

(8) A number of contradictions in irresponsible criticizm

   Some critics say, "TRON Project has no new concepts.", but also say "It has
no compatibilty with past software." The more compatibilities with past

softwares we have, then the more difficulties we may face to incorporate new concept.Isn't that a big contrdiction?

They have gotten angry with PC manufacturers who complain about the lack of users' efforts. In spite of this, they say that users do not accept TRON Concept(which comes from PC users' view point!)

They say that TRON Concept is not well accepted in foreign countries, but also say to the people who try to make TRON Concept understand in the world,"It must be in vain."

When a lot of people come to support TRON Concept, then such support may not become a NEWS.

There is a contradiction that the articles that no one knows or writes may be sold well.

So far, there have been many contradictions and misunderstandings about TRON Project because of lack of informations and its PR. In order to remove them, Dr. Ken Sakamura has been explaining and will continue to explain TRON Philosophy for years. I admire him for his great patience and devotion.

We are tring to inform as many people as possible what the exact TRON Project is so that, we hope, TRON Project as well as TRON Concept and TRON Culture will grow up more strongly by a lot of discussions .

6. The Realtime Operating System for Industrial Embedded System

It was an operating system for microprocessors that TRON Project studied from its very beginning. In 1983 Dr. Sakamura and a lot of companies in Japan Electronic Industry Development Association (JEIDA) collected the desirable functions of the realtime operating system for industrial embedded system as one of JEIDA activities. The definition of ITRON (Industrial TRON) specification which is now one of subprojects of TRON Project was done by several voluntary companies and is available for 8086, 80286MMU, 68000, 32032 and Gmicros today. μ ITRON specification for 8 bit single chip microcomputers has been recently added to those definitions. ITRON specification products are almost compatible with each other. The reason why we say almost is that some individual ITRON specifications related to each microprocessor are provided so as to obtain higher performance and to utilize the strong point of each microprocessor. Although there are many different kinds of operating systems available in today's market, it often happens that users have to develop their own one because the specifications of comercialized realtime operating systems often do not match with users' requirements. However, to make the matter worse, it is tough and sometimes difficult to transport the developed operating system from one microprocessor to another. That is because the development of an

operating system costs us huge amount of man-power.

Nowadays the technology development for semiconductor is being rapidly progressed and its speed is rather faster than that for software. A lot of microprocessors with attractive features are being introduced one after another.

Nevertheless, the developers are not free to use new microprocessors because of the existence of current operating systems and applicaton softwares which may not havecode compatibility with new microprocessors.

The operating systems defined by ITRON Concept can give users some clues to solve these problems.

(1) Some voluntary companies in TRON Project developed their own operating systems available for 68000, V Series, 80286 and proprietary microprocessors. In addition, since all of those application softwares are interfaced with ITRON specification OS in C language, those application softwares can easily be ported to the other ITRON specification operating systems. In short, it is thanks to C language and ITRON specification operating system that users can freely choose one microprocessors out of many different architectures.

(2) Since there are many companies who are developing ITRON specification OS for TRON specification 32 bit microprocessors, users can easily port their application softwares on current ITRON specification OS to future TRON specification 32 bit microprocessors.

(3) If we can use ITRON specification OS in combination with a TRON specification 32 bit microprocessor then we can expect to have highest perfomance possible for embedded system enviroment.

Hitachi is developing HI Series operating system for HI8, HI16, HI32 in addition to the development of HI68K(HI Sereis realtime operating system for 68000).Hitachi's HI Series realtime operating systems are based upon ITRON specification.

7. Business Use Operating System

8. Communication Control Operating System

Semiconductor Division of Hitachi Co., Ltd. does not actually take part in these two subprojects, so I refrain from reporting about them here.

9. 32/64 Bit Microprocessor

The ultimate purpose of TRON Project is to create 32 bit microprocessor with incorporating latest technology available in 1990's on which we can make the best use of ITRON or BTRON specification operating system. Before we finalize the specification of the 32 bit microprocessor it was very strong and intentional idea by Dr. Ken Sakamura that the 32 bit microprocessor should have

easy expansibility to future 64 bit archetecture although anyone actually spoke little of the necessity for future 64 bit address expansion for those days. Even today only a little people say the necessity to transfer to 64 bit address.

At present we have lively been developing 32 bit microprocessor in TRON Project. For example, three manufacturers (Fujitsu, Mitsubishi and Hitachi) have announced already Gmicro family products cooperatively developed with each other and Toshiba also has announced TX series development. I will not write about the detailed technology of 32 bit microprocessor but the main characteristics of its business.

(1) The First Success of Multi-Vendor for 32 Bit Microprocessors

Most 32 bit microprocessors available in the market are supported by a single sorce, so that the original manufacturers would fundamentally have to continue to develop peripherals or succeeding microprocessors alone even if they could have a second source. In TRON Project we have a quite different way of thinking of developing a 32 bit microprocessor. That is, each manufacturer may implement its own microprocessor with incorporating standard TRON archetecture. In case of Gmicro family, moreover, three manufacturers (Fujitsu, Mitsubishi and Hitachi) clearly divide microprocessor product range into three different levels, and each manufacturer develops in each range to exchange masks each other after the completion of those developments. Those three microprocessors will have a kind of family compatibility with others, so that users can freely select the favorite products out of microprocessor family. The most important point is that we will provide different level of performance, fanctionalities and cost ranges within the same architecture accordingly. Gmicro family including the possibility of future cooperated development would be only one of the clearest answers to those unlimitted expansion of users' requirements.

(2) The Sharing of the Development for Peripherals and Softwares

The three manufacturers take charge of the development for peripherals and support softwares other than microprocessor development. The shared developments are for a FPU(Floating Point Co-Processor Unit), DMAC(Direct Memory Access Controller), CACHE Memory, Interrupt Controller and so on. For the area of support softwares, those are an assembler, linkage editor, librarian, C-compiler, C runtime library, MPU/FPU Simulator, object file format converter, FORTRAN, PASCAL, COBOL, ITRON specification OS, UNIX, VME Board and so on. These tool developments include also the ones at third parties.

Other than VME board systems, we are also developing TOBUS(TRON BUS) specification.

(3) The Standard will be put into public domain

As well as ITRON specification, everyone can freely use the 32 bit microprocessor architecture when we complete the development and put those specifications into public domain. This is very important and basic spirit of TRON Project which fundamentally differs from the way of thinking which we have experienced in the other case of the industry by now. The companies or individuals who implement LSI's or softwares should have ownership of copyright or intellectual property for those products. The standard may contribute to the development of the industry with its free use by anybody.TRON Project is the first trial of establshing the standard among manufacturers before productizing of 32 bit microprocessors.

At present a lot of industries are greatly concerned about the developement of 32 bit microprocessors in TRON Project. We have been and will be making every efforts to promote its development and the more wide spread.

NOTE(1)   MS-DOS is the registered trademark of Microsoft Co., Ltd.

NOTE(2)   UNIX is the name of the operating system by AT&T Co., Ltd.

The BirliX Operating System

Gerhard Goos

German National Research Center for Computer Science (GMD)

St. Augustin

Abstract

The BirliX operating system uses the hardware scenario of networks, multiprocessor architectures, and large main memories to improve on reliability, security and performance. This paper is a summary of its objectives and main features. It concentrates on major aspects of distribution, reliability and security, and outlines the system's architecture. Based on an object oriented system interface, the Berkeley Unix (1) 4.3 system interface is emulated.

(1) Unix is a trademark of AT&T Bell Labs

CTRON Research and Development

Fukuya Ishino

Introduction

The use of computer technologies in communication networks has evolved steadily, both in demand and in the level of the technology employed. This can be attributed to such factors as the introduction of program-controlled switching systems, network digitization, and intelligent terminals, as well as progress in semiconductor technology, and even deregulation of the telecommunications industry.

As a result of this evolution, distinctions between communication systems and computer systems are becoming blurred. Requirements for realtime response and round-the-clock operation, which have long been common in telephone network control, are now being applied as well to computer systems in some cases, such as when computers are used in conjunction with switching systems to provide additional functions, or when computers are used in VAN nodes. Switching software designers now have to consider CSI protocols, which were originally developed for computer-to-computer communications. Many databases are commonly accessed from both switching nodes and computer systems.

CTRON is a set of software interfaces designed to meet this trend in future communication systems. The functional primitives described in CTRON specifications are aimed at creation of readily portable software that satisfies the demanding requirements of information communication networks in the 1990s and beyond. Below is a brief progress report on CTRON studies.

Design Objectives

CTRON defines interfaces between operating systems and application programs in network nodes. These interfaces are capable of supporting realtime response and round-the-clock operation. They are aimed also at improved software portability, making it possible to use the same software modules with different hardware.

Project Organization

CTRON studies are part of the overall TRON Project, being promoted by Dr. Ken Sakamura of Tokyo University, and funded by more than a hundred corporations worldwide. Work on the CTRON Technical Committee is carried out by about 200 engineers from nine companies: Fujitsu, Hitachi, Matsushita, Mitsubishi, NEC, Northern Telecom, NTT, Oki, and Toshiba. Membership on the CTRON Technical Committee includes the obligation by each company to support the project not only

by funding studies, but also by providing engineers, and developing and producing a minimum of one CTRON-based product.

The working groups under the CTRON Technical Committee are composed mainly of computer engineers and communication engineers. In some cases the support they receive from colleagues in the same field but in rival companies may be more cooperative than that provided by strangers in their own company but in other fields.

Interface Classifications
i) Hardware Dependency
CTRON interfaces are grouped into Base functions and Extended functions, based on the degree of hardware dependency. Base functions require different program implementation for different hardware architectures; each such program is called a Basic Operating System. An Extended Operating System, on the other hand, which is implemented on the Basic Operating System, provides extended functions in a way that is readily portable among different hardware systems.

ii) Application Dependency
A CTRON-based program does not necessarily implement all of the CTRON interfaces. The Basic Operating System interfaces

are composed of a kernel function group and an input/output handling function group. The Extended Operating System interfaces are composed of function groups for file management, database management, execution control, communication control, and switching control, and for operation and maintenance. Each function group defines a limited number of subsets, enabling users to select an interface set based on their functional and performance requirements.

iii) Operation Circumstance Dependency

Many communication nodes require operation and maintenance functions peculiar to their own circumstances. In the CTRON system, operation and maintenance programs are provided in the application layer. The CTRON operating system also provides primitive interfaces, such as for diagnostic probe or system reconfiguration control, allowing these peculiar functions to be added on.

Relation to Other International Standards

Where possible, CTRON adopts existing international standards, such as OSI, CCITT ISDN interface, and SQL. UNIX support is being studied by an independent working group outside the TRON Association. This group is attempting to design interfaces to allow UNIX programs to be run on CTRON systems.

Progress of CTRON Interface Design

Specifications have been published in Japanese and English for the kernel, input/output control, program execution control, file management, and communication control interfaces. Additional specifications are to be made available by April 1989, along with guides for designing fault-tolerant systems.

Progress of CTRON Implementation

Partial adoption has already been made of a CTRON interface in NTT's ISDN nodes. CTRON Basic Operating Systems will be available from a number of manufacturers next year. The overall CTRON interface design is also to undergo a process of evaluation and enhancement, based on comments now being collected by the CTRON Technical Committee, including feedback from the implementation groups. The TRON Association began offering document-based validation testing this month. Software-based validation is scheduled to begin next spring, before products are shipped by manufacturers.

Dipl.-Kfm. K. Gewald, Siemens AG, München

Abstract

X/OPEN An Open UNIX Environment

Considered by many to be the single greatest advance in computing,
with profound implications for the end user, open systems represents a
truly major breakthrough in the world of standards in information
technology. Spearheading the movement is the X/Open group, which was
founded in 1984 by five forward-looking European information systems
companies joined together to encourage the movement of applications
software between systems of different manufactures.

With membership now including 15 of the world's leading information
systems companies, X/Open's mission is to free users from the shackles
of proprietary systems, allowing them to choose freely from a wide
range of software and run it on the machine of their choice - based on
their own requirements for service, functionality and performance.
X/Open's achievement has been to agree a set of standard interfaces,
called the Common Applications Environment, which can be supported
in both the computer system and the software designed for a particular
business need. This means that applications software written to X/Open
specifications can be run on any computer system supporting the same
specifications.

The X/Open Group was formed as a non-profit organisation.
The group today includes AT&T, Bull, Digital Equipment Corporation,
Fujitsu, Hewlett Packard, IBM, ICL, NCR Corporation, Nixdorf AG,
Nokia Data, Olivetti, Philips, Siemens AG, Sun Microsystems and Unisys.
Between them, these members have already supplied some 70% of the world's
installed UNIX systems. All have agreed not only to adopt UNIX but
to the definition of a true portability specification common to all
their products, the Common Applications Environment.

X/open was founded to adopt and adapt existing international and de
facto standards. It does not create standards. Where existing standards
are not coherent or gaps exist among them X/Open's role is to
co-operate technically with relevant bodies to resolve these issues,
always with the end-user in mind. For example, in defining the
operating system for the Common Applications Environment, which
was to be portable across a range of hardware, no internationally
defined system existed. Unix, however was the de facto standard in that
area and already the base operating system for a wide range of
commercial, engineering, scientific and educational applications.
Originating in AT&T's Bell Laboratories, it was designed to be easily
adapted to many different types of machine. It was therefore chosen as
the basis for the X/Open operating system.

Over the next three years, the UNIX-based multivendor market is predicted to grow from 6% to 22% of the market by 1992, expanding at the rate of $ 7 billion a year. Such expansion is larger than the turnover of most of the companies that are in the IT business. In Europe, the UNIX-based market will grow to 16 times its present size by the end of 1991, according to figures released by Frost & Sullivan, with system sales rising from 40,500 to 677,000 systems during this period.

The X/Open Common Applications Environment comprises an integrated set of definitions, a mix of agreed National/International standards and widely accepted de facto standards. Although based on a standard operating platform, the Common Applications Environment embraces the many other services which the user (Business or Government) and applications developer need.

The basic modules of the Common Applications Environment are:

> Operating System Interfaces
>
> Programming Languages
>
> Data Management
>
> Interconnection
>
> User Interface

X/Open sees a vital part of its role as ensuring that it intercepts International standards as they emerge. The Group works closely with ISO (International Standards Organisation) committees through its members to ensure convergence of standards and avoid duplication of effort. An example of such co-operation is the emerging standard for operating systems known as POSIX. This is a step in taking the definition of the operating system away from any single computer system supplier and placing it firmly in the public domain. X/Open, as an institutional member of the Institute of Electronic and Electrical Engineers has played a major role in the definition of POSIX.

The IEEE 1003.1 Standard will be published in full-use form during 1988 as an American National Standard and as an ISO Draft International Standard (DIS). All the X/Open member companies have promised support for the POSIX standard.

POSIX addresses operating systems only, while X/Open is concerned with offering the user all aspects of multiple choice of systems, connectivity and true applications portability. Together, the two provide the user with real value.

ELECTRONIC PATENT APPLICATION SYSTEM BASED ON THE OSI CONCEPT

Tadasi Ishii
JAPANESE PATENT OFFICE

Introduction

In order to deal with ever increasing patent application and patent information, the Japanese Patent Office started a ten-year program in 1984 to construct a paperless system to proceed with all patent procedures from application to examination, as well as to furnish patent information to the private sector by computer.

The program is progressing satisfactorily, so far having succeeded in storing data for examination in the database and in developing a computerized search system. Electronic applications are expected to be accepted beginning in 1990. Electronic application will permit an application by flexible disc (FD) or on-line instead of the conventional paper application.

The computer system for the program is in fact extremely large in scale, requiring four host computers only for the initial system in 1990 and with a program scale of 3 million steps. Moreover, OSI is used as LAN protocol to interconnect computers as well as computers and workstations. OSI is also used as protocol for on-line application.

Concept of Electronic Application

The electronic application system will be introduced with the intention of accepting patent applications by flexible disc (FD) or by on-line using communication net work in addition to the papers. Electronic application starting from 1990 include patent and utility model applications, various intermediate documents.

When filing an application by flexible disc, it requires to store the application data in a disc in accordance with the standard specification set by the Patent Office. As in the same manner, it requires undergoing the formalities in accordance with protocol and format specification provided for in the standard specification when applying through on-line using a net work.

Very speedy and accurate application procedures can be anticipated by electronic application. For instance, an on-line application takes only about two minutes for its transmission and an applicant far from Tokyo can make application in a very short time. Moreover, the computer immediately indicates a fault, if there is any, in the procedure and so informs. Such step to now has required several weeks for the Patent Office to notify and inform about its correction.

Although far-reaching effects can be expected of electronic system, there are also many problems to be solved on the other hand. It requires, for example, the fundamental review of the

former legal system, which was constituted on the assumption of paper application only. The most important problem is system development for accepting electronic applications and automatically processing office procedures by computer. The system should also be developed in a manner enabling applicants to use the electronic application system.

System Architecture

Various functions are required for the electronic application system as well as in the internal system of the Office. The system is expected to handle a large volume of data (about six hundred thousand applications per year with each data length exceeding 100 KB), frequent exchanges of data and an absolute maintenance of security aside from the fact that the data content are in mixed mode (mixture of character code and image data). Under such conditions the system is to carry out complicated computer processing ranging from application to office procedures and from automatic edition of publication to database.

In order to carry out such advanced and complicated processing, the system was designed with independent sub-system for each function, which for their part, can localize problems when occurring. Moreover equipment was selected from plural makers so as to apply the optimum combination of machines for the required technologies. As such, the following concepts were adopted for the system architecture:

(1) The entire system is to be divided into sub-systems, with each sub-system equipped with host computer and file for independent operation.
(2) Sub-systems are to be connected by LAN with 100 Mbps.
(3) About 1,000 workstations are to be installed in the Patent Office and sub-systems and workstation are to be connected by separately installed 400 Mbps LAN.
(4) From the viewpoint of security, the on-line accepting system will be connected to two host computers as hot standby protection.
(5) The protocol overall will be unified.
(6) Optical discs are to be used for memory storing of electronic document originals to maintain security.
(7) ISO ODA/ODIF shall apply to the handling of mixed data.

Basic Concept of Information Network System

Since free access from various terminals is a precondition set forth for electronic application, an access method to the system using a specific protocol or any method limiting the operability of equipment is undesirable. As such, a standardized protocol is required .
The construction of a system connecting sub-systems poses a problem of connecting interfaces. Different type of interfaces

supplied by various makers necessitates a standardized protocol. In addition, the protocol should possess high performing function enabling processing of high-grade exchanges between/among sub-systems.

In conclusion, the protocol to be used for the paperless system requires satisfying the following conditions:

(1) It should permit an extension of the system, and should be based on a consistent concept over a long period.
(2) It should be in conformity with national and international standards.
(3) It should be highly efficient in processing huge amount of data in bulk and with precision.

After examining the above points, it was decided to adopt OSI entirely for the paperless system as its protocol and to merge the Patent Office's original protocol loaded with required functions for patent application and office procedures as a part of the application layer.

As its document format, it was also decided to adopt FDA (Formatted Document Architecture), which uses already fixed document file and is a part of ODA/ODIF (Office Document Architecture/Office Document Interchange Format) under standardization at the International Standardization Organization.

Structure of Protocol

The points considered for the structure of protocol are as follows:

(1) The protocol governing LAN in the Office and that for the electronic application are to be standardized with OSI, and the contents of sub-sets from the fifth layer to 7th are also standardized inside and outside of the Patent Office.
(2) ROSE is to be adopted for interactive communication classifying interfaces between/among sub-systems. Although the concept of ROSE is very simple, it is applicable to and powerful enough for the purpose of the paperless system. A part of P3 functions will be extracted for use as an argument of ROSE command. In addition, FTAM will also be used partly depending on the response promptness between host computers.
(3) The Patent Office's original protocol (Pp) takes precedence over shared application layers (ACSE/ROSE) and consists of the contents covering the details of envelope and document containing control information for transmission of documents.
(4) The Patent Office, in its conduct of service, requires a function to extract individual information at need. Therefore, a protocol will be adopted taking advantage of the partial functions of MOTIS and MHS, which are capable of identifying information communicated by header and body in the contents and characterizing the nature of information.

(5) As for the document format to be transmitted by on-line, a
     part of ODA/ODIF (Office Document Architecture/Office
     Document Interchange Format) standardized by the ISO and the
     one already fixed document file, FDA (Formatted Document
     Architecture) will be adopted.
(6) As for the networks, LAN (host, CSMA/CD· viewed   from
     terminals) will be used in the Office, ISDN and DDX-P will
     be used outside the Patent Office.

Conclusion

     The electronic application system among the paperless system
of the Patent Office has been completed in its main programming
part and is under connection test at present. The system
development is scheduled to be completed by the fall of 1989.
Thereafter undergoing an operation test period, the acceptance of
electronic application is expected to start in 1990.
     The   system includes many up-to-data technologies   and
especially the adoption of OSI as its protocol is worthy of note
in view of the system's scale and its wide range of application.
The positive adoption of OSI in its paperless program will no
doubt mark a new stage of OSI.

Fig. 3 Scope of message specification

Applicant's System

Data Entry System

Paper FO

Paper

DDX-P   ISDN

FO

Communication Control Processor

IU   Accepting System   IU

CSMA/CD (10 Mbps.)   IU

Accepting File

Terminal (for accepting etc.)

CSMA/CD (10 Mbps.)   IU   Clerical Processing System   IU

High Speed LAN (410 Mbps.)   High Speed LAN (100 Mbps.)

Assistant File   Fee File   Formality Check File

Application Data Management System   IU

IU

CTCS

* Publication Printing System

x   Publication Master File   Electronic File Wrapper

CSMA/CD (10 Mbps.)   IU   Publication   Current System   IU

IU

Terminal (for formality check etc.)   Comprehensive Data Base Search File   Current Terminal   Registration Master CTCS File

IU   Examination Comprehensive Document Data Base System

Terminal (for search, comprehensive document data base)

CSMA/CD:Carrier Sense Multiple Access with Collision Detection
CTCS:Channel to Channel System
IU:Interface Unit

Fig.1   CONFIGURATION OF SYSTEM

Layer	Governing protocol			
7	Pp: Paperless system particular protocol .... IS 8650 | DIS 9072			
6	IS 8823 IS 8824 IS 8825			
5	IS 8327 (kernel, full duplex)			
4	IS 8073 (class 0)			
3	I. 451	IS 8208	IS 8208	
2	I. 441	IS 7776	IS 7776	
1	I. 430		X. 21	X. 21 bis
Applicable network	D channel | B channel .... ISDN		DDX-P	

ISO (IS:International Standard   DIS:Draft International Standard)
7776   High-level data link control procedures
8073   Transport Protocol Specification
8208   x.25 Packet Level Protocol for DTE
8327   Basic Connection Oriented Session Protocol Specification
8650/2   Protocol Specification for the Association Control
            Service Element
8823   Connection Oriented Presentation Protocol Specification
8824   Specification of Abstract Syntax Notation One (ASN.1)
8825   Specification of Basic Encoding Rules for Abstract Syntax
            Notation One (ASN.1)
9072/2   Protocol Specification for Remote Operations

CCITT
I.430   Basic User Network Interface Layer 1 Specification
I.441   ISDN User Network Interface Data Link Layer Specification
I.451   ISDN User Network Interface Layer 3 Specification
X.21   Interface between DTE and DCE for synchronous operation
            on PSDN
X.21bis Use on PDNs of DTE which is designed for interfacing to
            synchronous V-series modems

Fig.2 Communication Protocol

OUTLINE OF PAPERLESS SYSTEM

Applicants and Representatives

Application Text

On-line
Floppy Disc
Paper
(to be electronized)

Office Action Text

On-line
Paper
(mailing)

Accepting System

Dispatching System

Accepting

Dispatching

Data Base of
ectronic File Wrapper

Administrative Data
(including
Bibliographic Data)

Application Data
(including Amendment
and Office Action)

Automated Compiling System for Publication

Publication
Data

Paper
Electronic
Publication

Data Transfer

Data

Public
Service

Paper
On-line
Electronic Data
(Optical disc
including CD-ROM)

Assistant System
for Office Action
Formality Check System
Inspection System

Clerical Processing

Clerical Processing
using Electronic Data

Examination
and Trial Examination

Search using
Retrieval Term. etc.

F-term Search System
D-term Search System
T-term Search System
J-term Search System

Comprehensive
Document
Data Base

Data Base
for Examinaton
(with Retrieval Term)

Public
Inspection

VDT-Paper

Local Reading Room

VDT-Paper

STEP TO PAPERLESS SYSTEM

			I 1984 – 86	II 1987 – 90	III 1991 – 93	Completion of Paperless System
Application & Clerical Processing	Form of Application		←————— Paper Applications —————→ (1990)		←——— Electronic Applications/Paper Applications ———	
	Data Base of Electronic File Wrapper			←Accumulation and Use of Administrative Data→	←Accumulation and Use of Electronic File Wrapper————	
	Clerical Processing System	·Processing System for Electronic Application [1]	Basic ←—System—→ System Design Design	←Programming→←—Trial—→ ←— Full Operation ————————		
		·The others	Basic ←——System—→ Design	←———————— Development and Enhancement ————————		
		·Administrative System	System ←—Design—→←——Programming——→	←Test→←— Full Operation ————		
Examination & Trial Examination	F-term Search System (Patent, Utility Model)		←Development and Trial of Basic System→ (F-term indexing in 180 Technical Field)	←—— Enhancement ————		←— Full Operation
	D-term Search System (Design)		←———————Development and Trial of Basic System———→	←—— Enhancement ——→		←— Full Operation
	T-term Search System (Trade Mark)			←———Development and Trial of Basic System———→	←—— Enhancement ——→	←— Full Operation
	J-term Search System (Trial Examination)		←———Development———→←——Full Operation———————			
Comprehensive Document Data Base			←——Accumulation of Domestic Publications (Patent, Utility Model)	←—Accumulation of other Domestic Publications and Foreign Publications		
Public Service			On-line Public Inspection at Patent Library and Osaka (Oct. 1986)	←——— Expansion ——————— On-line Public Inspection at Fkuoka (Jul. 1987)		

[1] including Accepting System and Formality Check System.

Flowchart on acceptance of applications

	Applicants or their patent attorneys	Accepting system
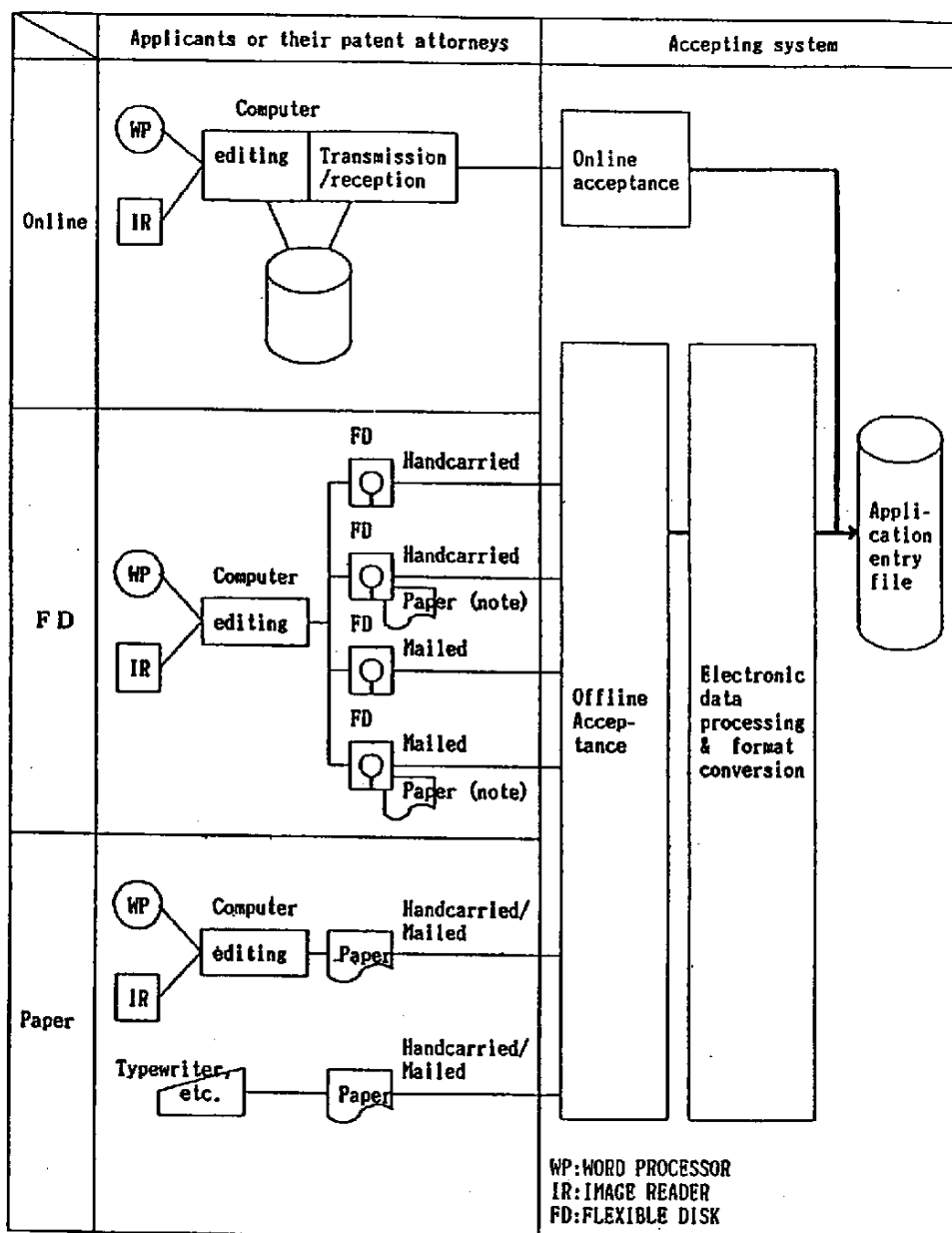
(note) Drawings, diagrams, etc.

WP: WORD PROCESSOR
IR: IMAGE READER
FD: FLEXIBLE DISK

JPO

Paper, mailed

Online

Paper, hand-carried

FD, hand-carried

FD, mailed
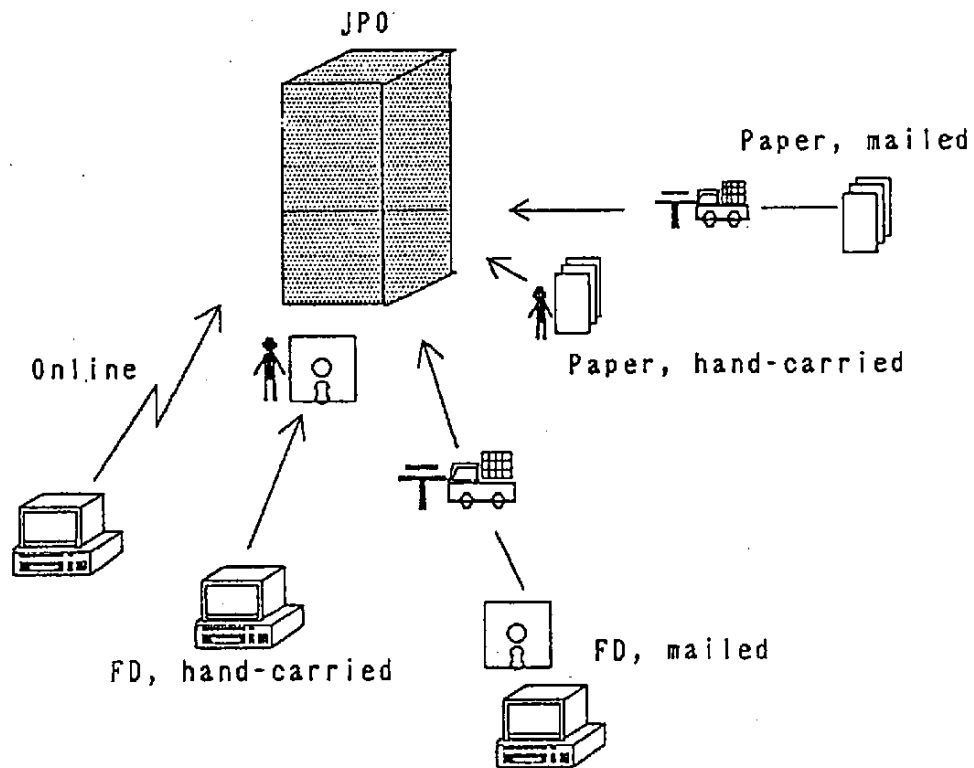
Computerized Application System

Applicant A   DDX－P

4800、9600bps

Patent
Office

Applicant B   I S D N

64Kbps
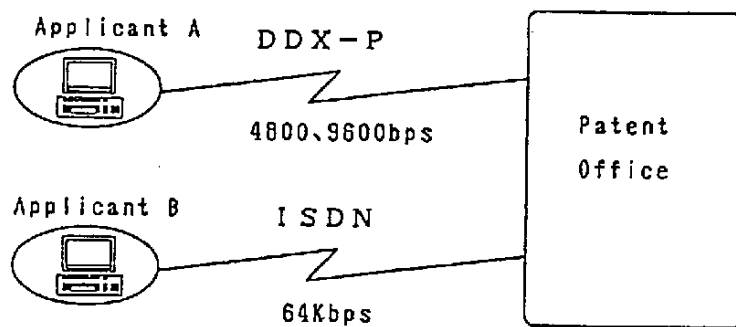
Data Transmission Lines for Online Application

Applicant's System

Data Entry System

Paper FD

Paper

OOX-P   ISDN

FO

Communication Control Processor

IU   Accepting System   IU

CSMA/CD (10 Mbps.)

IU

Accepting File

Terminal (for accepting etc.)

High Speed LAN (410 Mbps.)

CSMA/CD (10 Mbps.)   Clerical Processing System

IU   IU   High Speed LAN (100 Mbps.)

Assistant File   Fee File   Formality Check File

Application Data Management System

IU   IU

*Publication Printing System

CTCS

Publication Master File   Electronic File

Wrapper

CSMA/CD (10 Mbps.)

IU

Publication   Current System

IU   IU

Terminal (for formality check etc.)

Comprehensive Data Base

Current Terminal

Registration Master CTCS File

Search File

Examination Comprehensive Document Data Base System

IU

Terminal (for search. comprehensive document data bose)

CSMA/CD:Carrier Sense Multiple Access with Collision Detection
CTCS:Channel to Channel System
IU:Interface Unit

Fig.1   CONFIGURATION OF:SYSTEM

Layer	Governing protocol		
7	Pp: Paperless system particular protocol -- IS 8650		DIS 9072
6	IS 8823 IS 8824 IS 8825		
5	IS 8327 (kernel, full duplex)		
4	IS 8073 (class 0)		
3	I. 451	IS 8208	IS 8208
2	I. 441	IS 7776	IS 7776
1	I. 430		X. 21	X. 21 bis
Appli-cable network	D channel	B channel ISDN	DDX-P

ISO (IS:International Standard DIS:Draft International Standard)
7776   High-level data link control procedures
8073   Transport Protocol Specification
8208   x.25 Packet Level Protocol for DTE
8327   Basic Connection Oriented Session Protocol Specification
8650/2 Protocol Specification for the Association Control
          Service Element
8823   Connection Oriented Presentation Protocol Specification
8824   Specification of Abstract Syntax Notation One (ASN.1)
8825   Specification of Basic Encoding Rules for Abstract Syntax
          Notation One (ASN.1)
9072/2 Protocol Specification for Remote Operations

CCITT
I.430   Basic User Network Interface Layer 1 Specification
I.441   ISDN User Network Interface Data Link Layer Specification
I.451   ISDN User Network Interface Layer 3 Specification
X.21   Interface between DTE and DCE for synchronous operation
          on PSDN
X.21bis Use on PDNs of DTE which is designed for interfacing to
          synchronous V-series modems

Fig.2 Communication Protocol

Layer	Governing Protocol			
	Terminal - Host		Host - Host	
7	P p		F T A M	P p
	IS 8650	DIS 9072	IS 8650	IS 8650/DIS 9072
6	IS 8823 IS 8824 IS 8825			
5	IS 8327		IS 8327	IS 8327
4	IS 8073 (class 4)			
3	IS 8473			
2	IS 8802/2			
1	IS 8802/3			

Applicable network	LAN

Pp   :Paperless system particular protocol
IS   :International Standard
DIS   :Draft International Standard
FTAM   :File Transfer Access and Management
IS 8650 :ACSE   Association Control Servise Element
DIS 9072:ROS   Remote Operation Service
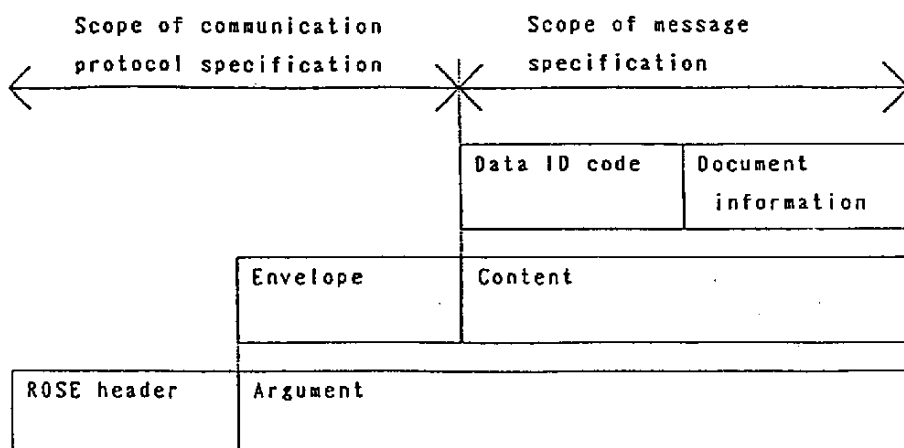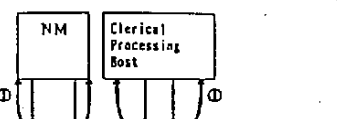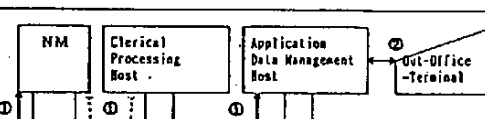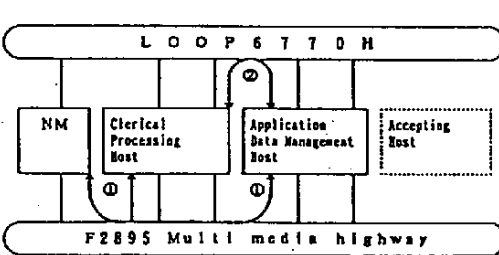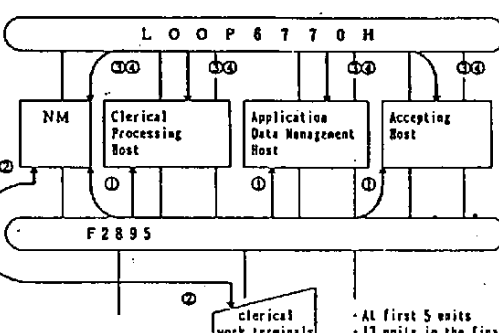
Fig. 3 Scope of message specification

Schedule	NETWORK CONFIGURATION	OUTLINE OF THE TEST
1988 Jul. 4 ↓ Jul. 14	[NM] [Clerical Processing Host] ① ① ① — Connecting NM and Clerical Processing Host to coaxial cable by Jul. 4. coaxial cable confirmation test on Jul. 4.	Confirmation test of local adjustment and actions, and preparation for the tests by Jul. 4. ①Return Test via coaxial cable of NM and Clerical Processing Host.
Jul. 15 ↓ Aug. 7	[NM] [Clerical Processing Host] [Application Data Management Host] ① (In the course of SG) — Start of connection test of NM with Clerical Processing Host from Jul. 15.	①Fp Protocol Test (normal pattern) – the test by the interface of coaxial cable (CSMA/CD). – NM-to-Clerical-Processing-Interface Test.
Aug. 8) ↓ Aug. 14	[NM] [Clerical Processing Host] [Application Data Management Host] ② [Out-Office -Terminal] ① ① ① — Connecting Application Data Management Host to coaxial cable on Aug. 8.	①Fp Protocol Test (normal pattern) – the test by the interface of coaxial cable (CSMA/CD). – NM-to-Application-Data-Management interface (Practiced by connecting the cable between Clerical Processing and Application Data Management) ②Out-Office-Terminal Connection Test. (Fp Protocol Test normal pattern)
Aug. 15 ↓ Sep. 9	L O O P 6 7 7 0 H ② [NM] [Clerical Processing Host] [Application Data Management Host] [Accepting Host] ① F 2 8 9 5 Multi media highway — Connecting every host to Branch-Line-LAN (coaxial cable) on Aug. 15. (Connecting the system to Host-LAN and Terminal-LAN.)	①Fp Protocol Test (normal pattern) – via Terminal-LAN – NM-to-clerical-processing-interface Test and NM-to-Application-Data-Management-interface Test. ②Transport Layer Protocol Test (normal pattern) – via Host-LAN – Clerical-Processing-to-Application-Data-Management-interface Test.
Sep. 10 ↓ 1989 May.	L O O P 6 7 7 0 H ③④ ③④ ③④ ③④ [NM] [Clerical Processing Host] [Application Data Management Host] [Accepting Host] ② ① ① ① F 2 8 9 5 ② [clerical work terminals] · At first 5 units · 13 units in the final stage (NTT, Shinagawa) — Connecting Accepting Host and clerical work terminals to LAN on Sep. 10.	①Fp Protocol Test from Sep. (abnormal pattern) – via Terminal-LAN. ②Fp Protocol Test from Sep. (normal and abnormal pattern) – NM-to-Clerical-Processing-interface-Test – via Terminal-LAN. ③Transport Layer Protocol Test from Oct. (abnormal pattern) – via Host-LAN. ④FTAM Test from Oct. (normal pattern) – via Host-LAN.

Intelligent Interfaces for Knowledge-Based Application Systems: The Combination of Language, Vision and Graphics in Multimodal Systems

Wolfgang Wahlster

Computer Science Department, University of Saarbruecken

6600 Saarbruecken 11, F.R.G.

(01149)-681-302-2363

wahlster%fb10vax.sbsvax@sbsvax.uucp
wahlster%sbsvax.uucp@germany.csnet

A multimodal user interface is one that supports more than one medium through which users and application programs can communicate. For example, such an interface might support graphics, gestures, natural language, menus, sketching and video. An intelligent interface is one that exploits knowledge about the task, the application, and the user in ways that help the user accomplish the interaction goal efficiently. The basic technical prerequisites for multimodal interfaces are fulfilled (high-resolution bit-mapped displays and window systems for the presentation of visual information, various pointing devices such as mouse, light-pen, joystick and touch-sensitive screens for deictic input, the DataGlove or even image sequence analysis systems for gesture recognition). But the remaining problem for artificial intelligence is that explicit meanings must be given to multimodal interactions, eg. in terms of a formal semantics of the visual world.

In face-to-face conversation humans frequently use deictic gestures parallel to verbal descriptions for referent identification. Such a multimodal mode of communication is of great importance for intelligent interfaces, as it simplifies and speeds up reference to objects in a visualized application domain. Natural pointing behavior is very flexible, but also possibly ambiguous or vague, so that without a careful analysis of the discourse context of a gesture there would be a high risk of reference failure. The subject of this talk is how the user and discourse model of an intelligent interface influences the comprehension and production of natural language with coordinated pointing, and conversely how multimodal communication influences the user and discourse model. After a brief description of the deixis analyzer of our XTRA system, which handles a variety of tactile gestures, including different granularities, inexact pointing gestures and

pars-pro-toto deixis, we present some empirical results of an experiment, which investigates the similarities and differences between natural pointing in face-to-face communication and simulated pointing using our system. We show how gestures can be used to shift focus and how focus can be used to disambiguate gestures. We discuss the impact of the user model on the decision of the presentation planning component, as to whether to use a pointing gesture, a verbal description, or both, for referent identification. Then we present anticipation feedback as a particular method of user modeling, which can help the system to select the right granularity of a presentation when generating multimodal output.

We review previous research on multimodal user interfaces and describe some current projects related to our work, currently being carried out at the FhG, the GMD and an industrial consortium funded by the BMFT. Finally, we discuss the relation of the current project to the scientific program of the German AI Center in the area of intelligent user interfaces.

International Online Banking Systems in Japan

Yoshiaki Iwamaru

Chief Researcher and Consultant

Mitsui Research Institute

4-10, Nihonbashi-Honcho 3-chome, Chuo-ku, Tokyo 103, Japan

1. Introduction

In Japan, the financial industry is playing a leading role in computerization and in establishing network systems. Keeping up with the development of its banking systems, the industry is one of the forerunner of future Japanese information society. During the last two decades, banks in Japan have developed large online information network systems, which are generally classified into two generations. And now, they are just developing the third generation systems.

Hereafter, I will describe about the development of Japanese banking systems briefly, and then, international information systems along with the third generation banking systems.

2. Development of Banking Systems in Japan

In 1965, the first online banking system in Japan started its operation. A few years later, other banks followed suit to develop their online banking systems. These first generation systems covered services for each type of deposit independently, such as ordinary deposits, current accounts, time deposits, etc. The intra-bank network systems were also developed to offer online services among headquarters and branches for respective banks. Also cash dispensers (CD's in short) were introduced, first in off-line mode (1969), and then in online mode (1971).

In the decade starting from mid-1970's, next generation of online

$-150-$

systems was developed, to integrate banking applications including deposits, domestic exchange, loans and foreign exchange businesses. CD's were enhanced into multi-purpose automatic tellers machines (ATM's in short), which handle not only withdrawals but also deposits and remittances.

In the decade starting from mid-1980's, many banks have introduced or are developing, so-called third generation systems. New systems offer electronic banking services for corporate and individual customers through these networks. Services for international banking business are re-organized also, and new systems are planned for information services and decision supporting. The third generation systems are the strategic ones for respective banks. Therefore each bank's system looks somewhat differently in certain points. Some of them are enforcing information services for their own banking operations; others are forcusing for interconnection with customers. In general, new systems are said to be consisting of six components, as follows:

    banking operations support system
    information systems for headquarters and branches
    electronic banking systems for firms and customers
    bond and treasury systems
    international business and communication system
    distributed branch operation support system

3. Development of Network Systems

The first step for networking was to install intra-bank network systems. Using these network systems, 'network service deposit' and 'bank-card' deposit services were offered. Domestic exchange and data communication system for all banks were introduced early in this decade, and called 'Zengin System.'

In the second step, inter-bank CD network systems were introduced. The Nippon Cash Service was established for joint use of CD's, through joint investment by city banks, regional banks and sogo banks totaling 54 in 1975. Other atttempts for joint utilization of CD's were launched in 1980.

    Six   city   banks' CD service (SICS) in May
    Seven city   banks' CD service (IOCS) in April
    71   sogo banks' CD service (SCS) in October
    63 regional banks' CD service (ACS) in October

Later, trust banks' CD service (SOCS) was introduced. SICS and TOCS were

-151-

combined into new 13 city banks' CD service (BANCS). Today, it is planned that BANCS and ACS will be integrated into one large CD network system, and some of other CD networks will also join into the new one.

International network systems were introduced in this decade. Each bank developed its own branch systems for foreign branches. These branch systems are linked into the headquarters systems through communication networks. Also, banks in Japan joined S.W.I.F.T. network in 1981.

In the third step, banks access to their customers directly, and for customers, vice versa. Through telephones, videotex, facsimile and personal computers, firms and individuals can refer to and update database directly. And these networks are going to expand connection with other network systems (VAN).

4. International Banking Systems

In general, banking systems for foreign branchs can be classified into three categories.

① stand-alone branch systems
② regional center network systems
③ host centralized systems

Currently, many banks have international banking systems to be cassified in type ①. Functions are added for communicating with host systems, switching to S.W.I.F.T., CHIPS, and other systems (fig.). Recently, on the other hand, Japanese banks are studying feasibility for grading up their systems. Some possibilities are functions for managing global multi-currency applications, and 24-hour global operation facilities.

5. Conclusion

Importance of global banking operations is rapidly increasing, and thus new concept for international system is being needed. As domestic systems are in the course of completion, Japanese banks are in a position to start new projects for development of international online banking systems.

FIGURE OF INT'L BUSINESS SYSTEMS
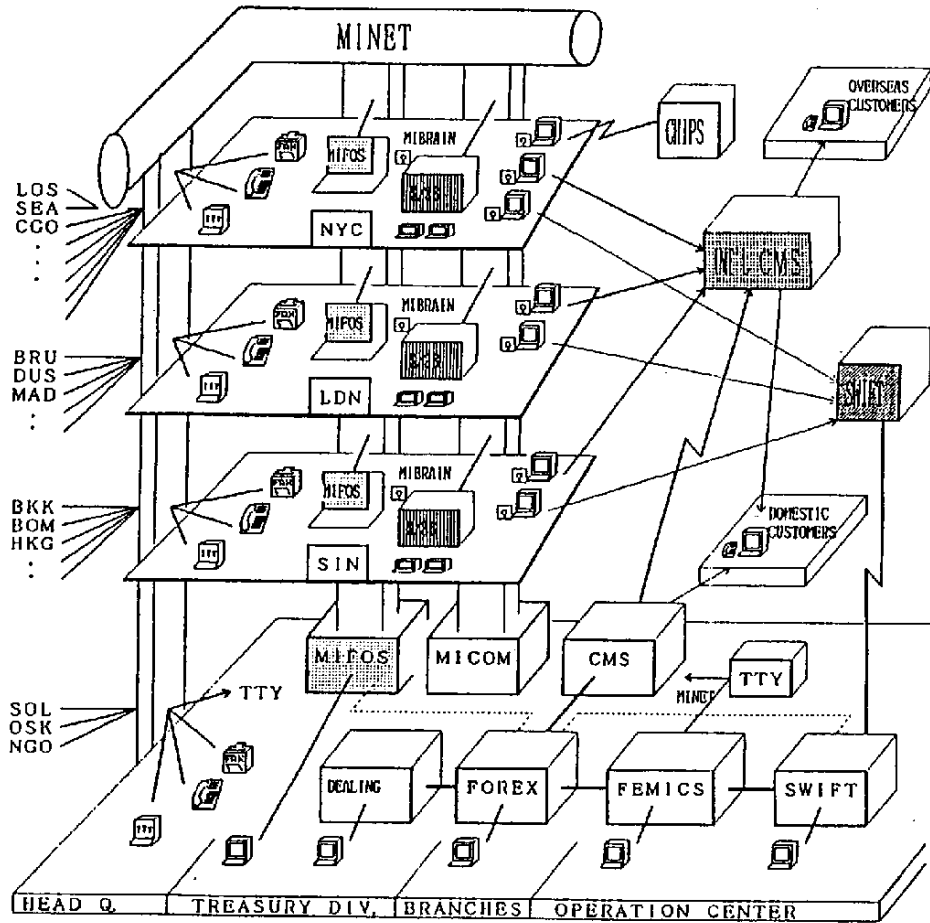
MINET   : Mitsui Int'l NETwork
MIFOS   : Mitsui Int'l Funds Online System
MICOM   : Mitsui Int'l data COMunication
MIBRAIN   : Mitsui Int'l BRAnch INhouse system
FEMICS   : Foreign Exchange Mitsui Computer System

Dr. Hans Delfs
Wolfram Howein

Erlangen, 1.08.1988
SIEMENS AG
Systemtechnische Entwicklung

Benefits of knowledge based techniques in industrial automation

Due to the growing complexity of industrial automation configuration, installation, operation and maintenance of automation systems are becoming more and more sophisticated tasks. The volume of documentation is increasing steadily. The navigation through different documents (e.g. manuals, operating instructions, handbooks ect.) to solve existing problems is expensive and time consuming. This leads to a rapidly growing demand for computer assistance in this field. The application of advanced techniques and tools from Artificial Intelligence can contribute essentially to the solution of these problems. This can be shown by the success of various knowledge based systems developed at the Energy and Automation group of Siemens.

Major problems in maintenance are the lack of human experts and the transfer of knowledge from experienced field engineers to junior engineers. They are addressed by an expert system tool which supports the systematic acquisition of knowledge in a problem-oriented way. The knowledge is used for diagnosing faults in technical systems, e.g. speed controlled dc drives. Applications implemented with this tool include an extensive documentation of diagnosis and background knowledge. The documented knowledge is linked to the underlying diagnosis hierarchy and may be retrieved in a "hypertext way". The system presents to the user those pieces of knowledge which are relevant in the current state of diagnosis.

Another typical example of an expert system serves as an intelligent assistant in the (now semiautomatic) configuration of distributed automation systems based on multi-microcomputer systems.

Techniques like rule processing, object oriented programming or frame-based representation of structures today already belong to the more classical methods in Artificial Intelligence. Though sometimes called the "weak methods", they prove to be quite strong in our complex applications. Their availability marks real progress in software technology.

To our opinion a lot of basic research is still required until the more advanced concepts in expert system technology like qualitative reasoning on physical models can be widely applied to real problems in automation.

There is at least one problem with most of the existing AI-software-tools today. It is difficult and sometimes even impossible, to integrate them in existing applications or to deliver efficient run time systems on the hardware used in our offices and factories today. The reason is that most tools either are ideally adequate for rapid prototyping, based on languages like Lisp or Prolog and therefore require a lot of computing power (a typical example is KEE) or they do not fully support the flexible combination of various problem solving techniques (necessary to solve the problem). So one goal of our activities is to develop a modular toolbox on top of the language C which fits into our conventional data processing environment.

System Architecture for Highly Parallel Systems

Karl Solchenbach

SUPRENUM GmbH, Hohe Str. 73, D-5300 Bonn

Gesellschaft für Mathematik und Datenverarbeitung, D-5205 St. Augustin

Summary

Supercomputer architectures

Today many different approaches for a classification of computer architecture, especially with respect to parallel processing, are discussed. A classification may be based on quantitative aspects (the degree of parallelism or the granularity), the structure of the control-flow (SIMD, MIMD, data-driven, demand-driven), the (hardware) technology (VLSI, VHSIC, air cooled, liquid cooled, see [1]), or the topology of the processing elements and the memory units.

From the application programmer's point of view the most important classification categories are:

1. SIMD vs. MIMD,

2. shared vs. distributed memory,

3. scalar vs. vector floating point units.

A more elaborate motivation of these categories and a description of the resulting classes of super- and parallel computers is given in [2].

The SUPRENUM hardware

SUPRENUM is a German supercomputer development characterized by the following architectural properties:

- highly parallel (256 nodes)

- powerful nodes (MC68020 CPU, a fast floating-point vector unit (8 Mflops peak performance, 16 Mflops with chaining), fast vector memory, DMA, communication coprocessor;

- local memory (8 Mbytes on each node);

- cluster structure (each cluster contains 16 nodes, a disk, a diagnosis node, and a communication node);

- two-level bus system (clusterbus 256 MB/s, SUPRENUMBUS 25 MB/s).

The Abstract SUPRENUM architecture

The user's view of the system is the *Abstract SUPRENUM architecture* which is based on a dynamic process concept which is characterized by the following elements:

- Processes are autonomous program units which run in parallel.

- Processes communicate only by exchange of messages, and no shared memory is available.

- In arithmetic expressions and communication instructions, array constructs are especially supported.

- The user defined process system is homogeneous and independent from the actual hardware configuration. The two-level architecture (cluster structure) is not reflected in the Abstract SUPRENUM architecture and is completely transparent to the user. The processes are mapped to the clusters and nodes at run-time.

The Abstract SUPRENUM architecture is the central model in the system software. The user should write his codes only in terms of processes.

The programming language for numerical computations is SUPRENUM-Fortran, an extended Fortran 77. The extensions include special process handling and message-passing

constructs and an array syntax formulation according to the proposed Fortran-8X standard.

A set of tools is provided to support the deveopment of parallel programs (performance analysis, simulator, debugger, syntax based editor, vectorizer, parallelizer, etc.)

The application software

The availability of practical relevant application software is decisive for the scientific and commercial success of a new computer architecture. This software must, of course, make use of the specific advantages of the architecture and translate these advantages into gains of speed.

- Basic solvers

  The basic numerical software available on SUPRENUM consists of

    - a parallel Linear Algebra package (similar to LINPACK/EISPACK),

    - some solvers for basic partial differential equations (PDEs) using highly efficient parallel multigrid (MG) algorithms,

    - a package for ordinary differential equations.

- CFD applications

  The emphasis within the application software development lies on computational fluid dynamics (CFD) codes. These cover most of the standard CFD models used today including potential, Euler, and Navier-Stokes models.

- Other applications

  Besides the CFD applications many different application software packages are either developed or parallelized for SUPRENUM during project (Finite Elements, oil reservoir simulator, reactor safety simulations).

The design of the SUPRENUM system was largely influenced by the algorithms and data structures used in the applications. As an example, we consider CFD simulations on block-structured grids. The SIMD/MIMD architecture of SUPRENUM corresponds exactly the local fine grain parallelism (vectorization) in each block and the coarse grain

parallelism on block level. The communication network of SUPRENUM guarantees a fixed communication distance (independent of the system size) and supports algorithms with non-local communication patterns (like multigrid).

Estimates show that for realistic aerodynamical simulations a sustained performance of more than 1 Gflops will be achieved.

References

[1] Giloi, W.K.: SUPRENUM – a trendsetter in modern supercomputer development. In [4].

[2] Solchenbach, K., Trottenberg, U.: SUPRENUM – System essentials and grid applications. In [4].

[3] Trottenberg, U.: The SUPRENUM project: idea and current state. Proceedings of the SPEEDUP Workshop on Vector and Parallel Computing in Berne, 15 Jan. 88, to appear.

[4] Trottenberg, U. (ed.): Proceedings of the 2nd International SUPRENUM Collo-qium "Supercomputing based on parallel computer architectures". Parallel Comput-ing 7, North Holland, 1988.

A Semantic network machine: IXM

Tetsuya Higuchi
Electrotechnical Laboratory
1-1-4 Umezono, Tsukuba, Ibaraki 305, Japan

Introduction

Semantic network is a knowledge representation scheme which uses *nodes* to represent concepts and *links* to represent the relationships between concepts. For example, two nodes and one link are used in Fig.1 in order to state a knowledge that the vintage year of Chablis wine is 1976.

Semantic network representation is very easy to understand the herarchical structure of knowledge and so it has been widely used in areas of artificial intelligence such as knowledge base systems, human memory models and natural language processing.

However, in spite of its usefulness, applications using large semantic networks for practical use have not been developed so far. This is because the amount of computation explodes abruptly as the size of the semantic network grows larger. Conventional computers can not utilize the intrinsic parallelism in semantic network processing to reduce the processing time. The explosion of the search space is an inevitable problem in artificial intelligence and many algorithms of this nature can not be utilized fully due to the restriction of computational power.

In order to improve these circumstances, the authors propose a massively parallel hardware based on large associative memories for semantic network processing.
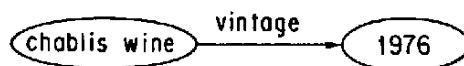
Figure 1: Semantic network

Semantic Memory System: IX

The IXM machine is the main component of the semantic memory system, IX [iks]. We are developing the IX system in order to support all the aspects of semantic network processing in an integrated fashion: from modelling and description of applications with the semantic network language IXL, to parallel execution of the IXL programs by the massively parallel hardware IXM.

IXM

Figure 2 shows the overview of the IXM machine. IXM accepts an IXL command for queries or generations of semantic networks, one at a time from the host computer. So all the PEs in IXM executes an IXL command in SIMD manner. But, during the execution of an IXL command, each PE operates in MIMD manner, independent of other PEs.

IXM consists of PEs and the associative network. Large semantic network to be processed by IXM is divided into sub-semantic networks. Each sub-semantic network is stored in associative memories of a PE where most of semantic network processings are done in parallel utilizing associative memories. PE has the other kind of associative memories to store the codes for IXL interpreter. The associative network consists of network processors(NPs) connected each other in a shape of tree structures or hypercube structures. NPs are used to send messages among PEs and to perform parallel marker propagations.
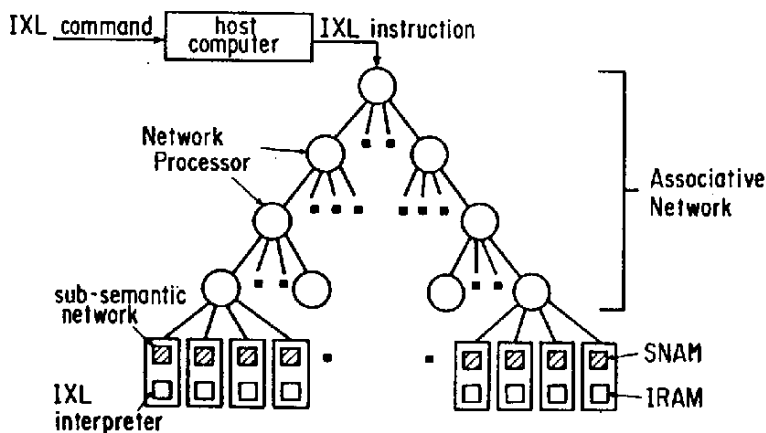
Figure 2: Overview of IXM

Semantic network processing

Machines for semantic network processing have to be able to execute three fundamental operations very efficiently: *associative operation, set operation,* and *marker propagation.* For example, suppose that there are two sets represented in the semantic network in Fig.3 and a query is issued to get the intersection of these two sets. In order to make the processing more efficient, we associate a set of one-bit flags with each node. These bits are called *marker bits.*
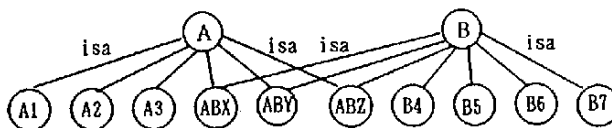
Figure 3: Representation of two set with semantic network

Using these marker bits, semantic network processing is done effectively as follows. At first node A is found with the associative operation. Then each member of set A can be reached by traversing along *isa* links from node A. Each member of the A set is marked by seting maker bit No.1 of each node. Similarly, each member of set B is marked with marker bit No. 2. As the markers propagates among nodes, these are called marker propagations. The nodes in which both marker bits No.1 and No.2 are set are the intersection of the two sets. So, AND set operation is broadcast to all the nodes in order to get the answers.

Associative memories can execute these fundamental operations very efficiently. In IXM machine, a link of semantic network occupies a word in associative memories. Each word consists of identifier field, destination field, link name field, and marker bits field. For example, the *isa* link between node A1 and node A in Figure 3 is represented on associative memory as shown in Figure 4(a). In order to set marker bits No.1 of all the members of set A, we firstly set the search register like Figure 4(b) and issue the search instruction to associative memories. Then the hit flag of each member's word is set in parallel as the result of search instruction. After this, we issue a parallel write instruction setting marker bits No.1 of the words which have been just searched by previous instruction. So, it take only 4 associative memory cycles to get all the members of set A: two for setting a search mask and a write mask, one for the search instruction, and one for the parallel write instruction. As long as all the set are contained in the associative memory, it is 4 cycles every time.

identifier	destination	link	marker bits

A 1	A	isa	0	0	· ·	0

(a)

masked	A	isa	masked

(b)
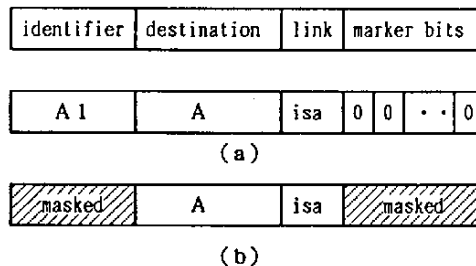
Figure 4: The representation of a link on the associative memory

The prototype of IXM machine

Figure 5 shows the overview of IXM prototype consisting of 32 PE boards and communications network(5 communication boards and a broadcasting board). It will be completed this December.

The host computer of IXM prototype is SUN3/260. The IXL language is incorporated into Quintus Prolog on SUN3 as user-defined predicates. So IXM prototype operates as the hardware accelerator of Prolog. It is also possible to incorporate into Lisp machines.

IBM PC/AT is also used as host computer for the development of IXM programs and for the debugging.
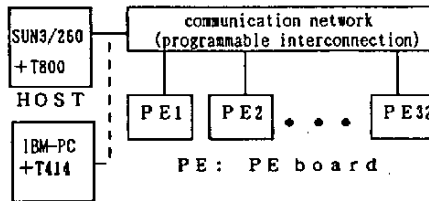
Figure 5: Overview of IXM prototype

PE: PE board

The PE board consists of 4Kword X 40 bit associative memory, Inmos T800(17.5 MHz), 4 communication links, and 128Kbyte SRAM, as shown in Figure 6. A PE board has 8 connections with other boards through communications boards. Communication boards are programmed to establish arbitary interconnection topology among 32 PE boards. Access time of the associative memory is 230 ns, but the cycle time is about 400 to 500 ns as the associative memory has independent clock and is accessed asynchronously by T800. The programs for operating IXM are written in Occam2: IXL language interpreter, monitor, etc.

Figure 6: PE board

AM: Associative Memory
A-bus : address bus
LA: link adaptor
I-bus : instruction bus
D-bus : data bus
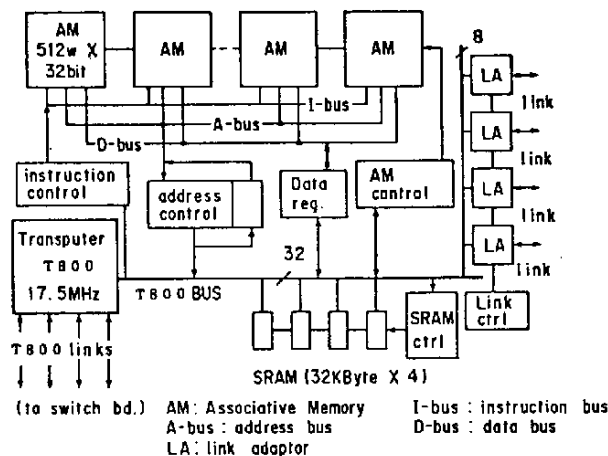
Conclusion

AI programs for practical uses involve massive parallelism. However, most of them remain untouched due to the lack of parallel architectures. The authors will investigate these problems with the IXM prototype which has parallelism over 100000 when all the associative meories are installed.

References

[1] S.E.Fahlman: *Design sketch for a million NETL machine* , Proc. of First Annual National Conf. on AI, 1980.

[2] K.Handa, T.Higuchi, A.Kokubu and T.Furuya: *Flexible Semantic Network for knowledage Representation*, Journal of Information Japan, Vol.10, No.1, 1986.

[3] T.Higuchi, T.Furuya, H.Kusumoto, K.Handa and A.Kokubu: *The IX supercomputer for knowledge based systems*, Fall Joint Computer Conference, November 1986.

A Semantic Network Machine: IXM

Tetsuya HIGUCHI
Electrotechnical Laboratory
1-1-4 Umezono, Tsukuba, Ibaraki 305, Japan

Semantic Network

- representation scheme using links and nodes
  a node $\Rightarrow$ a concept.
  a link $\Rightarrow$ a relation between two concepts.

Applications

- natural language processing

- knowledge based systems

- human memory models

Problems

execution time of large semantic networks
$\Longrightarrow$ explosion of search space

IX system

- A total knowledge information system based on semantic networks

- IX system provides,

    - IXL: a semantic network oriented knowledge representation language
    - IXM: parallel hardware to execute IXL programs

Objective of IX

support of all the processes in semantic network processing in an integrated fashion;
from the modelling in SN, to the parallel execution by IXM

Contents

1. IXL language

2. IXM architecture

   - semantic network processing
   - IXM overview
   - design features
   - performance estimation

3. Prototype of IXM

Knowledge Representation Language IXL

Functions

1. Description of SN

2. Deductive inference

Syntax

To connect nodes by a link:
link(is_a, X, Y).
link(not_isa, X, Y).
link(instance_of, X, Y).
link(a_kind_of, [X,Y,..], Z).
link(source, R, X).
link(destination, R, Y).
link(rule, X, ((
.. asst(R, X, Y) :- ...
.. prop(R, X, Y) :- ...
.. isa(X, Y) :- ...
.. instance(X, Y) :- ...)).

To construct a relation:
assertion(R, X, Y).
property(R, X, Y).

To inquire about a link:
isa(X, Y).
instance(X, Y).
ako(X, Y).
source(R, X).
destination(R, Y).

To inquire about a relation:
asst(R, X, Y).
prop(R, X, Y).

System-supported primitive links:
is_a, not_isa, instance_of
not_instanceof, a_kind_of,
source, destination

Three main features of IXL

1. User-defined relation represented not by a link but by a network of nodes

```
 ( chablis wine ) --vintage--> ( 1976 )

 ( wine ) <--source-- ( vintage ) --destination--> ( year )
    ^                     ^                            ^
    |isa                  |isa                         |isa
 ( chablis wine ) <--source-- ( ○ ) --destination--> ( 1976 )
```
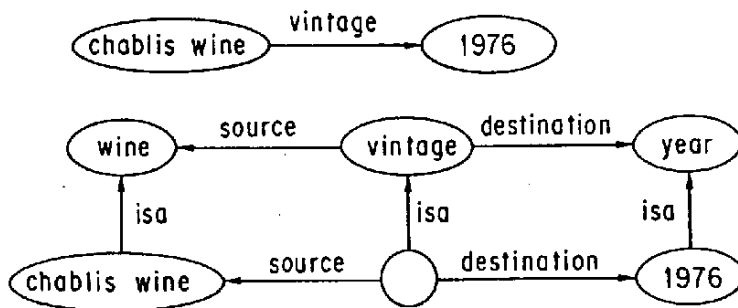
2. procedure addition in logic like expression

isa(X, high_class_restaurant) :- asst(entree, X, Y),

asst(main_dish, X, Z),

$Z + Y > 100.$

3. negative knowledge explicitly described

IXM architecture

Semantic network processing

- Fundamental operations are:

    1. associative operation
    2. set operation
    3. marker propagation

- Utilization of marker bits assigned to a node

Example: Who belongs to both A and B group?
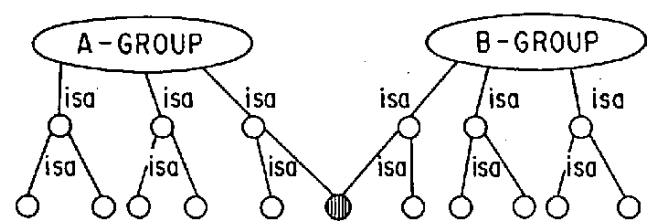
IXM architecture

- ### Associative Network
  4-ary tree structure with a Network Processor(NP) at each node

- ### Processing Element (PE)
  PE includes two associative memories:
  - Semantic Network Associative Memory (SNAM)
  - InstRuction Associative Memory (IRAM)
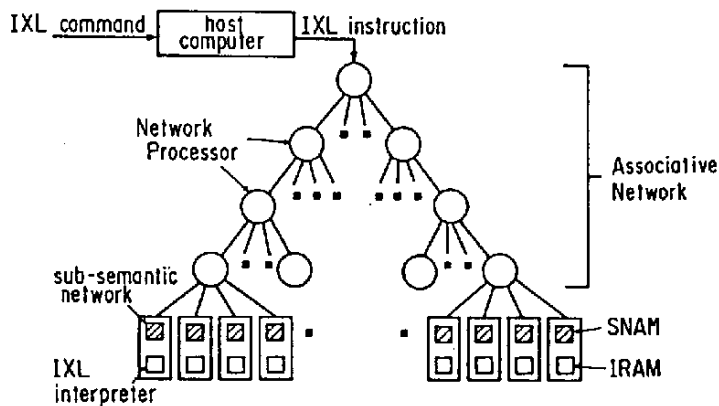
Execution of an IXL command

1. Input of an IXL command
2. Broadcast by host (SIMD)
3. Executions in PEs (MIMD)
4. Collection of answers
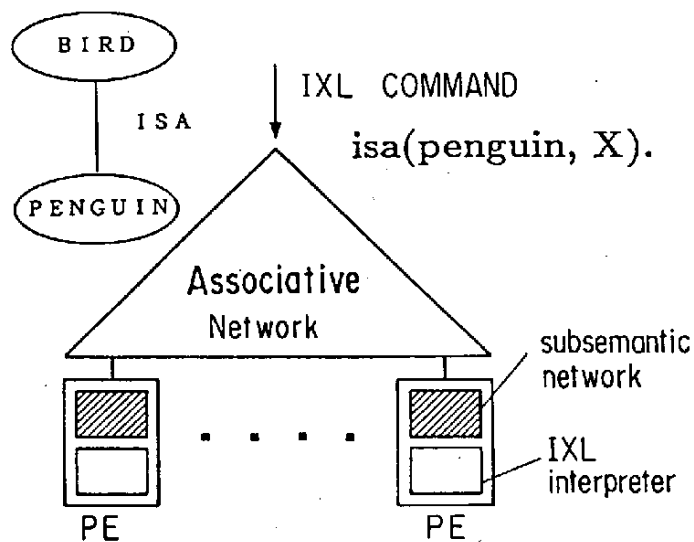
Design features (1)

Asynchronous IXM machine instructions

An IXM machine instruction becomes executable when a particular marker bit is set.

$\Longrightarrow$An answer is sent to the host as soon as it's found.

(If all the PEs are synchronized during the execution of an IXL command, turn around time becomes much longer.)

$\Longrightarrow$Marker driven mechanism

Example: (suppose a penguin is a bird)

- IXL command: isa(penguin, X).
- Subroutine of IXM machine instructions:

assoc(penguin, 1)
mark(1, isa, 1)
return(1)
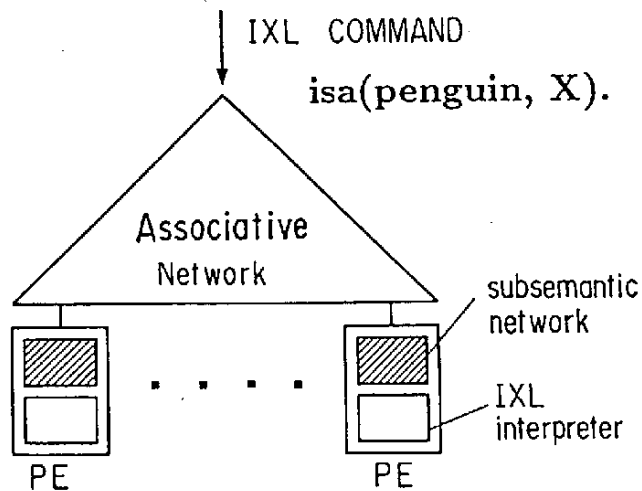
Design features (2)

Node of Equivalence for parallel marker propagation

- A node with many fanouts is a bottle-
  neck in marker propagation.
- Division of such a node
  into *nodes of equivalence*
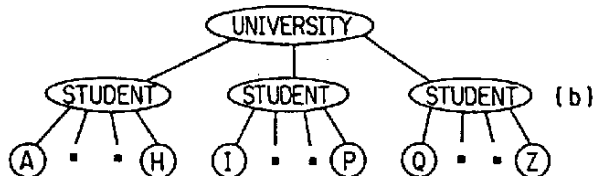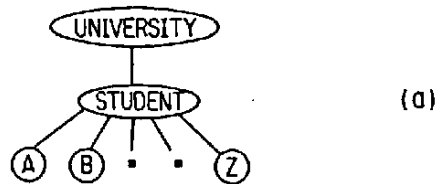
Parallel marker propagation
by associative network

If a marker is sent to one of *nodes of equiv-alence*, it has to be duplicated and sent to the other *nodes of equivalence.*
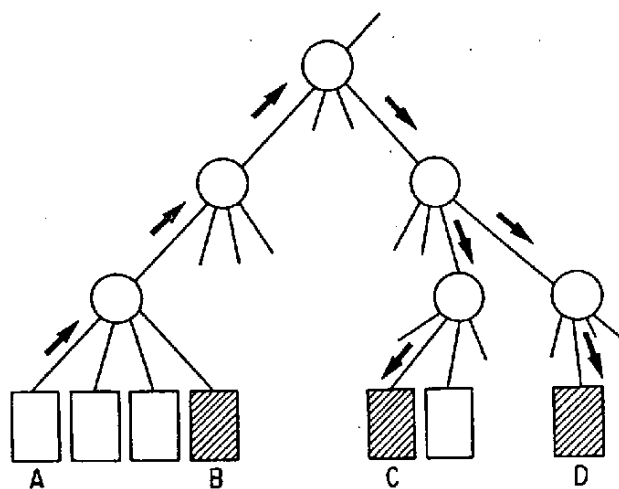
Design features (3)

Associative memory to store and process semantic networks

Associative memory potentially exploits the parallelisms,
in **associative operation** and
in **set operation**.
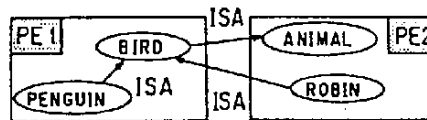
IDF	DSF	LN	MBF
BIRD	PE2(1) ANIMAL	ISA	·
BIRD	PE1(4) PENGUIN	RISA	·
BIRD	PE2(2) ROBIN	RISA	·
PENGUIN	PE1(1) BIRD	ISA	·
SNAM1 (PE1)			

ANIMAL	PE1(1) BIRD	RISA	·
ROBIN	PE1(1) BIRD	ISA	·
SNAM2(PE2)			

Performance estimation

- IXL written in K-Prolog on Micro VAX

KB size	1600 links	3300 links	4500 links
query 1	66 - 600 msec.	66 - 1183 msec.	66 - 1633 msec
query 2	2.1 min.	8.7 min.	14.6 min.

- Simulation of IXM (micro sec.)

KB size	1600 links	3300 links	4500 links
query 1	156	211	240
query 2	245	276	356

- query (1): usual database search
  query(2): deductive inference

- assumption:
  6 MByte/sec transfer between NPs,
  300ns associative memory

Prototype system

Purposes

1. Evaluation of the architecture
2. Experiments on connection topology
3. Execution of large semantic networks

Components

1. **Host computer**
2. **32 Processor boards**
3. **5 Communication Boards**

Processor board

(to switch bd.) AM: Associative Memory   I-bus : instruction bus
                 A-bus : address bus   D-bus : data bus
                 LA : link adaptor
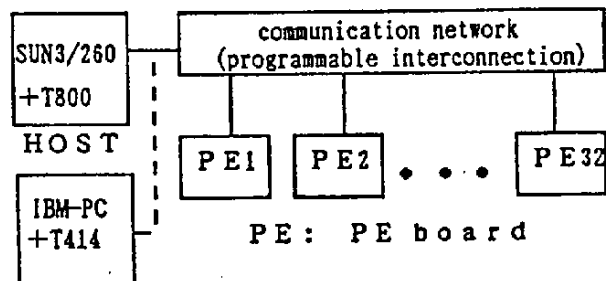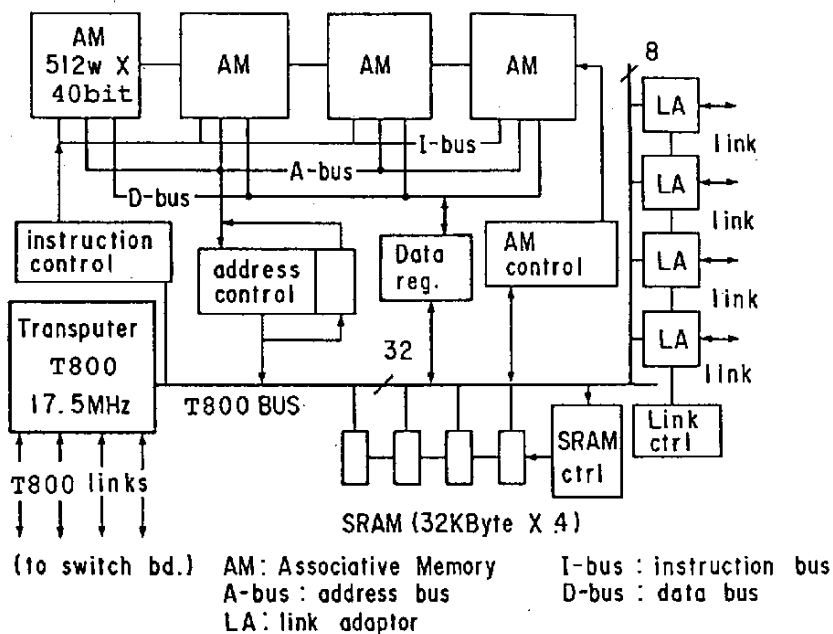
· Transputer 17.5 MHz, 8.5 MIPS,
        4 serial links, on-chip 2K PAM
· Associative Memories
    32bit X 2K words , 230 ns access time

Representation of a link
on associative memory

marker bits

		0 1 2 3 4 5 6	
identifier (ex. A)	link (iso)	0	1 st. word
destination (ex. B)	literal	1	2 nd. word

0   15   23   31

example :   (A) —iso→ (B)
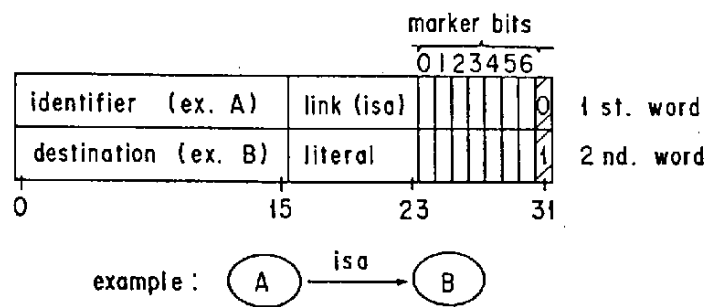
Conclusion

- Utilization of associative memory (AM)

  * AM in PE for associative and set operations
  * AM in PE for IXL interpreter
  * AM in NP for parallel marker propagation

- Study on allocation algorithms of SN

- Communication bandwidth

- Prototype will be operational next year.

A Parallel-Operating Prolog Computer

W. K. Giloi

Director, GMD Research Center of
Innovative Computer Systems and Technology
Research Professor of Computer Science,
Technical University of Berlin and
University of California at Los Angeles

Abstract

An architecture is presented for the parallel execution of sequential Prolog. The architecture is based on a pipeline of unification processors which work as co-processors to a UNIX based workstation. The unification processors execute highly optimized, compiled Prolog code; however, the basic concept of the architecture could also increase the performance of interpreter based systems. Parallel execution exploits the organizational parallelism as well as the AND parallelism inherent in Prolog programs. It can be shown that even programs that do not exhibit any of the 'classical' forms of parallelism (AND and OR parallelism) can be effectively mapped onto the proposed architecture. The presented architecture may also function very effectively as a multi-user Prolog machine executing several independent Prolog programs in parallel. In contrast to other attempts to execute sequential Prolog in parallel, we do not restrict the use of any of the standard Prolog language features such as dynamic assert/retract, CUT, etc. Simulation results show that peak execution rates of over 1000 KLIPS can be obtained. The system accepts standard sequential Prolog (e.g., DEC20-Prolog), which then is internally parallelized by the compiler. The compiler also employs a new, very efficient "hybrid" scheme of data dependence analysis, in order to exploit AND parallelism and perform "intelligent backtracking".

Computation in Neural Nets

W. v. Seelen, Biophysics Department, University of Mainz

As a rule, neural nets compare the weighted sum of the input
with a threshold and then weight the result non-linearily. Such nets
can be coupled with each other in layers and are suitable for
instance for multidimensional optimization, learning and image
processing. If such layered structures are specified and enhanced
with two-dimensional mapping and spatially discrete combination
of several parameter fields, then one gets systems that are
easily adapted to applications involving orientation in natural
three-dimensional surroundings.

付録 4　半導体分科会アブストラクト

MMICs for 30GHz-band Satellite Transponder

Haruhiko KATO

NTT Radio Communication Systems Laboratories
1-2356, Take, Yokosuka-shi, Kanagawa-ken, 238-03 JAPAN

1. Introduction

Satellite transponders must be extremely lightweight and highly reliable. Monolithic microwave ICs (MMICs) have great potential for fulfilling these requirements. However, most MMIC development has remained on a small-scale, basic functional level in the Ka-band, and no examples of MMIC application to satellite transponders have been provided.

This article describes the outlines of MMIC development in NTT and their application to satellite transponders.

2. Fully implemented MMIC transponder configuration

The configuration of an MMIC transponder is shown in Fig. 1. To realize the full implementation of MMICs in a transponder, it is necessary to develop technologies which can remove narrow-band filters and dielectric resonators and to suppress the phase noise of MMIC oscillators. This is because filters occupy a large area on IC chips and limit their usable frequency range, while MMIC oscillators have fairly noisy spectra due to low Q characteristics. These problems have been solved by developing the phase shift-type image rejection mixer and by employing high speed phase lock technology in local oscillators. The hatched boxes in Fig. 1 are components in which MMICs are adopted. All the circuits of the transponder are implemented by MMICs except for the TWTAs and X'tal reference oscillators.

3. Key MMICs[1][2]

All the key MMICs needed to construct a 30/20GHz-band full MMIC transponder have been developed. The MMICs employ 0.3μm or 0.5μm gate length GaAs FETs with via-holes. The substrate thickness is 150um. The FETs used in this work were fabricated on GaAs VPE wafer with an active layer of 2-4 x 10^{17} cm^{-3} carrier concentration. Electron-beam lithography technology is employed for gate forming. The MIM capacitor insulator is Si_3N_4. Photographs of the developed MMICs are shown in Fig. 2.

3-1 30GHz two-stage amplifier

Lumped constant MIM (metal-insulator-metal) capacitors are employed as matching elements in the 30GHz two-stage amplifier. These provide a smaller circuit than conventional circuits that employ fully distributed-constant elements. MIM capacitors show wide capacitance deviation owing to fabricated insulator thickness deviation. The 30GHz amplifier presented here compensates for the deviations by novel circuit design. A typical gain of 5dB and a noise figure of 6dB have been obtained in the 27- 30GHz range. (Fig. 2(a))

3-2 30GHz image rejection mixer

The 30GHz image rejection mixer is composed of two single balanced mixers using Schottky barrier diodes and an active IF 90 degree hybrid. The active IF hybrid includes no distributed constant elements. A total signal to image ratio of 15-20dB and a conversion loss of less than 8dB have been obtained in the 27-30GHz range. (Fig. 2(b))

3-3 30GHz frequency doubler

An FET 30GHz frequency doubler is employed. The optimum termination for the input frequency at the output port was set to attain high isolation and high conversion efficiency. A conversion loss of less than 5dB and an input signal suppresion of more than 10dB have been obtained in the 26-32GHz range. (Fig. 2(c))

3-4 15GHz analog frequency divider

A Miller-type 15GHz analog frequency divider has been developed. A wideband characteristic of 14-16GHz has been obtained. (Fig. 2(d))

3-5 15GHz voltage controled oscillator

The developed 15GHz voltage controled oscillator is a varactor tuned full MMIC type without an external resonator. An ultra-wideband tuning range of 3GHz was obtained by a novel out-of-band damping resister circuit. (Fig. 2(e))

4. MMIC Modules[3]

Multi-chip type MMIC modules have been developed to make the MMICs easy to handle while maintaining compactness. The developed MMIC modules are shown in Fig. 3. Each MMIC module contains four to six MMIC chips and does not include any trimming circuits.

5. Full MMIC receiver[4][5]

One of the 30GHz-band fully implemented MMIC receiver shown in Fig. 1 has been assembled using the MMIC modules plus 1GHz IF amplifiers[6] and a 7.5GHz digital frequency divider[7]. Figure 4 shows a manufactured receiver breadboard. It weighs 200 grams, 1/6 that of a conventional hybrid IC receiver of the CS-3[8]. Various tests required for space equipment, such as temperature and electro-magnetic compatibility tests were carried out. The test results confirmed it is satisfactory for use in a satellite transponder system. Frequency response of the receiver from the 30GHz input to the 1 GHz output port is shown in Fig. 5. A sufficiently flat response of less than ± 1 dB was obtained in the frequency range of $f_0 \pm 200$MHz. The measured phase locked local oscillator output spectrum is shown in Fig. 6. A good SSB phase noise performance less than -80 dBc / Hz at 1kHz offset has been obtained.

6. Conclusion

30GHz-band MMICs and MMIC modules were succesfuly developed. A receiver was manufactured using the MMIC modules. The complete MMIC receiver presented here is being installed in transponders of the ETS-VI satellite (Engineering Test Satellite VI) that Japan intends to launch in 1992.

7. Acknowledgement

The author wishes to thank H.Fuketa, H.Yamamoto, T.Sugeta and T.Ohira of NTT radio communication systems laboratories for their valuable suggestions and encouragement in the MMIC development and its space applications, and M.Ohara and M.Suzuki of NTT LSI laboratories for supplying the newly developed IF amplifier ICs and digital divider ICs.

References

[1]   H.Kato et al.,"MMICs for Ka-band Multi-beam Satellite Transponder", *GLOBCOM '87* Tech. digest, pp.947-951, 1987, Tokyo.

[2]   T.Ohira et al.,"Development of Key Monolithic Circuits to Ka-band Full MMIC Receivers", *IEEE 1987 Microwave and Millimeter-wave Monolithic Circuits Symposium*, pp.69-74, June 8-9, 1987, Las Vegas.

[3]   T.Ohira et al.,"A Compact full-MMIC module for Ka-band phase locked oscillators", *IEEE Trans. Microwave Theory Tech.* to be published.

[4]   T.Ohira et al.,"MMIC 14GHz VCO and Miller frequency divider for low-noise local oscillators", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp.657-662, July 1987.

[5]   H.Kato et al., "A 30GHz-band full-MMIC Receiver for Satellite Transponders", *1988 MTT-S* Tech. digest, pp.565-568, 1988, New York

[6]   N.Ishihara et al., "GHz-band High Gain GaAs Monolithic Amplifiers using Parallel Feedback Technique", *1988 Symp. on VLSI circuits*, Aug. 1988, Tokyo.

[7]   M.Suzuki et al.,"A 9GHz Frequency Divider using Si Bipolar Super Self-aligned Process Technology", *IEEE Electron Device lett.*, vol. ED-6, No. 4, pp.181-183, Apr. 1985.

[8]   M.Tanaka et al.,"30/20GHz and 6/4 Band Transponder Development for Communications Satellite CS-3", IEEE 1986 ICC Tech. digest, pp.507-512, Toronto.
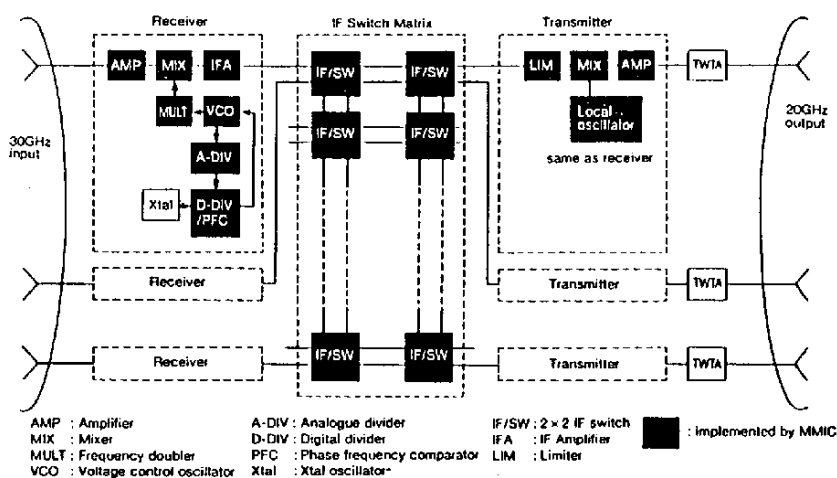
Fig. 1 MMIC Transponder Configuration
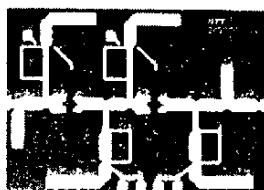
(a) 30 GHz two-stage amplifier
(2.2 x 3.07 mm)
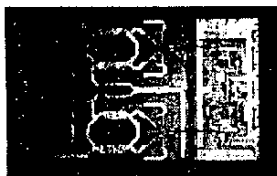
(b) 30 GHz mixer
with active IF hybrid
(3.5 x 5.7 mm)

(c) 15 GHz voltage controlled oscillator
(2 x 2.4 mm)
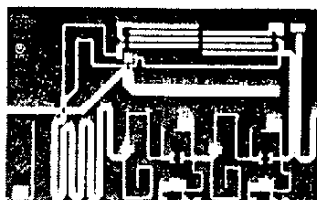
(d) 15 GHz analog frequency divider
(4.0 x 6.3 mm)

(e) 30 GHz frrequency doubler
(2 x 3 mm)

Fig.2 Key MMICs developed for Transponders
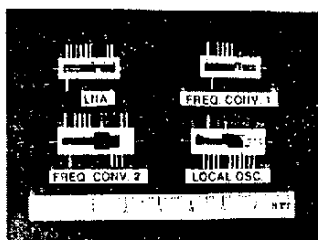
LNA: 30GHz low noise amplifier
FREQ. CONV. 1: non-image rejection
                   freqency converter
FREQ. CONV. 2: image rejection
                   freqency converter
LOCAL OSC.: local oscillator

Fig. 3 MMIC modules developed

left: receiver of the CS-3
right: MMIC receiver developed

Fig. 4 MMIC receiver
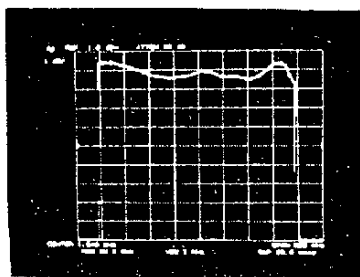
Input signal:30.805 GHz ± 200 MHz
Center frequency: 1.045 GHz
        H: 50 MHz / div
        V: 1 dB / div

Fig.5 Measured frequency responce of receiver
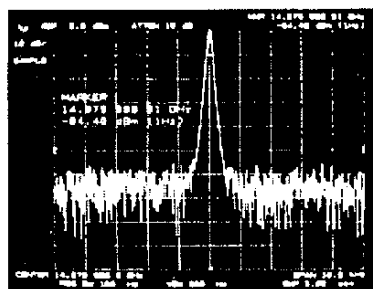
Center frequency: 14.88 GHz
        H: 100 Hz / div
        V: 10 dB / div

Fig. 6 Local oscillator spectrum

Development of GaAs mm-Wave ICs

H. Dämbkes*, A. Colquhoun**, E. Menzel***, B. Adelseck***

* AEG Research Center, Sedanstr. 10, D-7900 Ulm, FRG
** TELEFUNKEN electronic GmbH, Theresienstr. 2, D-7100 Heilbronn, FRG
*** AEG Radio and Radar Systems Division, Sedanstr. 10, D-7900 Ulm, FRG

For a growing number of different applications communication systems in the millimeter wave region are of high interest. Some areas are

- traffic guiding systems
- automotive radar applications
- high resolution imaging radar
- civil and military avionic radars
- fixed and mobile communication links
- sensing systems

Availability of integrated circuits containing at least the essential subsystems on one chip will reduce overall cost, increase reliability, reduce the size of these systems and will thus increase the chances for the new system in the market.

AEG is presently developing a set of chips for integrated receiver circuits, concentrating on the 35 GHz, 60 GHz and 90 GHz regions.

In a standard receiver circuit as shown in Fig. 1, oscillator, mixer, amplifiers, and filters are used. In a first step a monolithic integrated 35 GHz receiver chip was developed, consisting of a single balanced mixer and a single stage IF-amplifier. This is presently extended to 60 GHz circuits, including a low noise HEMT preamplifier and an FET-oscillator. The paper will essentially concentrate on the 35 GHz circuit and results obtained so far.
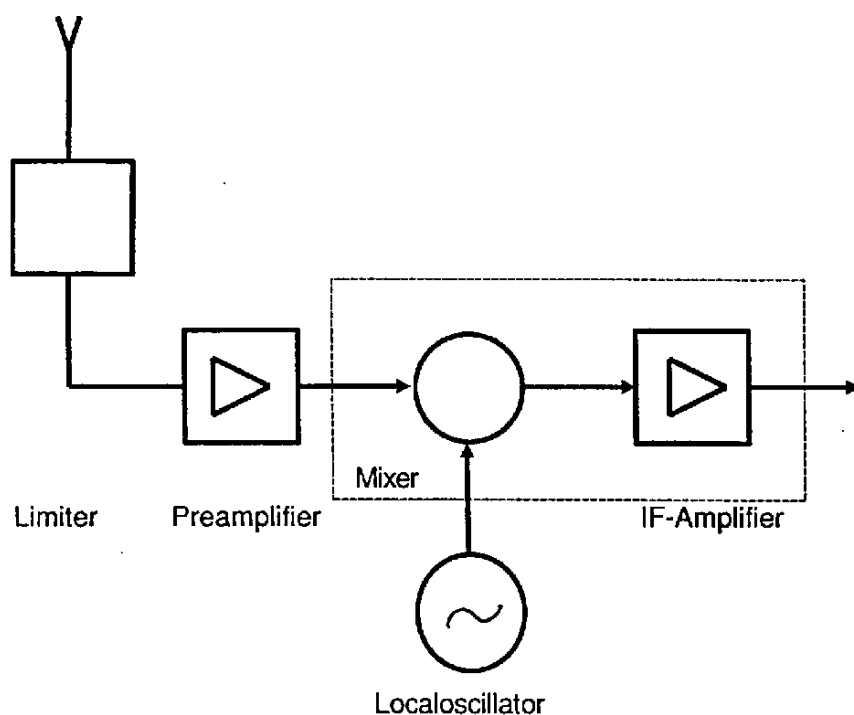
Fig. 1: Schematic receiver circuit

Fig. 2: The 35 GHz receiver circuit

MIXER DIODE   MESFET

SiO2/
Si3N4

Au   n   Au   Au

n+   n+   n+

Semi-insulating GaAs
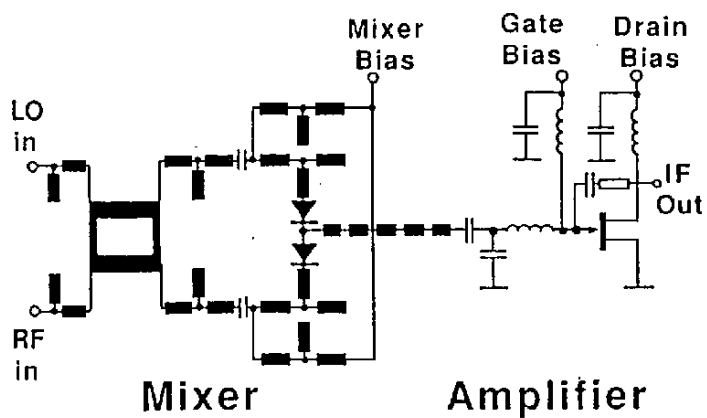
Boron   Schottky   Ohmic
Implant   contact   contact
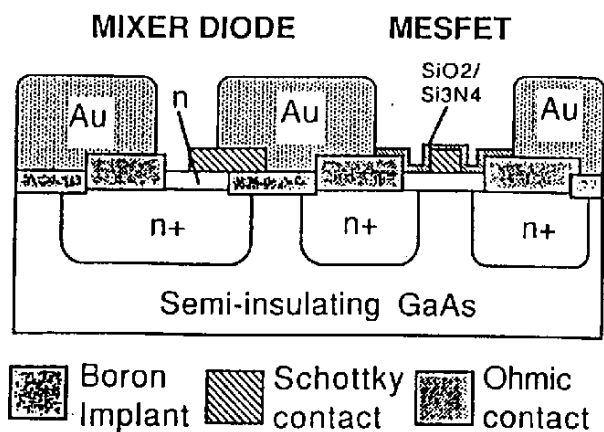
Fig. 3: A schematic cross-section of the active devices in the technology
        used for the 35 GHz receiver circuit

Hetero FET Inductor Diode Resistor Capacitor

semiinsulating GaAs
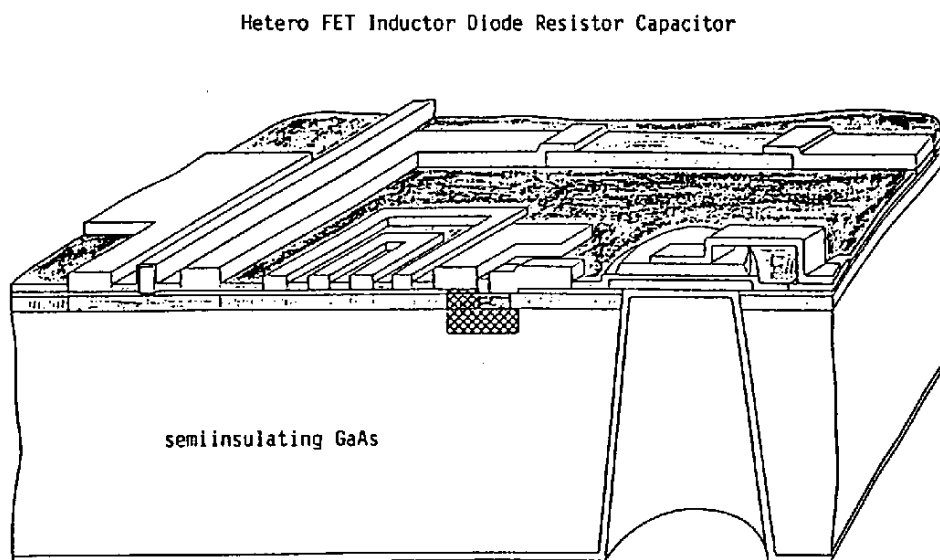
Fig. 4: A schematic cross-section of circuit using heterostructure FETs.

MILLIMETER-WAVE TRANSMITTER/RECEIVERS AND THE DEVICES

Yoshio OHGUSHI

(NEC Corporation)

Abstract

1.INTRODUCTION

Developmental efforts on the millimeter wave technology have
started in about 1970 in Japan for the wave guide transmission
system named W-40G. Since then,many systems have been developed
in several application fields by using the millimeter-wave
technologies which have many features as small size, large
transmission capacity, longer transmission distance than the light
wave and so on. This paper describes the technology of the
transmitter/receivers (TRXs) for these applications and the
millimeter wave devices used in the systems.

2.MM-WAVE TRX FOR SATELLITE COMMUNICATIONS

MM-wave satellite communications systems have been developed by
using Japanese communication satellite such as CS (1977,30/20
GHz), ECS (1980,35/32 GHz), CS-2 (1983,30/20GHz)and CS-3
(1988,30/20GHz). And recently, development of the millimeter wave
personal communications system and the millimeterwave
intersatellite communications system have been started to perform
experiments by using ETS-6 (Japanese Experimental Test Satellite
No.6). Figure 1 shows a block diagram of the mm-wave TRX equipped
on-board the satellite for this system. Devices such as a solid-
state high power amplifier (0.5 watts at 38 GHz) and a low noise
amplifier (4.8dB NF at 43 GHz) have been developed.

3.MM-WAVE TRX FOR PLASMA DIAGNOSIS

In order to measure the electron density of the plasma in JT-60 (Japanese Tokamak type fusion reactor for research),a millimeter-wave(140GHz) interferometer shown in Figure 2, has been developed. Ten watts EIO(Extended Interaction Oscillator) is used in the transmitter and a harmonic type GaAs Schottky barrier diode mixer is used in the receiver.

Electron temperature other than electron density can be obtained by measuring electron cyclotron emission power spectrum of the plasma.   For this measurement, a millimeter-wave spectrometer covering 110GHz to 260GHz is being developed.

4.MM-WAVE TRX FOR ATOMOSPHERIC TRANSMISSION MEASUREMENT

Atomospheric transmission characteristics of millimeter-wave are necessary for the transmission system design. In order to study the characteristics ,several experiments have been performed by using millimeter-wave transmitter/receivers in several millimeter-wave frequency ranges such as 50GHz,80GHz 103GHz,140GHz and 240GHz. Figure 3 shows a block diagram of 80/240GHz measuring equipment. As this TRX has two frequencies being coherent with each other ,not only attenuation difference but phase difference between two frequencies after atomospheric transmission can be measured.

Scattering characteristics of millimeter-wave from air , ground,building etc.is also important for designing the system being immune to interference. The Communications Research Laboratory has a four years plan from next year to perform the experiment on scatter in the frequency region of 50 to 100GHz.

5 MM-WAVE DEVICES

In order to satisfy the system requirement, the following devices have been developed.

1)InP FET

Millimeter-wave AlGaAs Hetero-MIS Gate InP FET was fabricated by using MBE and selective ion-implantation process. At 38 GHz, 8.1 dB small signal power gain ,showing cutoff frequency of 100 GHz, was obtained by 280um gate width and 100 mw output power by 420 um gate width.

2)LNA module

Two types of low noise amplifier modules have been developed for Ka-band(32 GHz) and O-band(43GHz) transponders equipped on-board the ETS-6. Frequency band ,noise figure and gain of the 32GHz Amp module and the 43GHz Amp module are 32.555+0.15GHz, 4.1 dB,15.6 dB and 43+0.05 GHz,4.8 dB,13.3 dB,respectively.

3)IMPATT Amplifier

Figure 4 shows output power of the IMPATT diodes having been developed in NEC. Dotted line shows developmental target. As a recent result, a pulse operational IMPATT has been confirmed to generate the target power shown by the dotted line at near 100 GHz.

4)GUNN Oscillator

Figure 5 shows output power of the GUNN diodes having been developed in NEC. Dotted line also shows developmental target power.

Fig.1 Configuration of 43/38GHz TRX
for Satellite Communication

Fig.2 Configuration of 137GHz TRX for Plasma Diagnosis

Fig.3 Configuration of 80/240GHz TRX
for Atomospheric Transmission Measurement

Fig. 4 Output Power of IMPATT Diode

Fig.5 Output Power of GUNN Diode
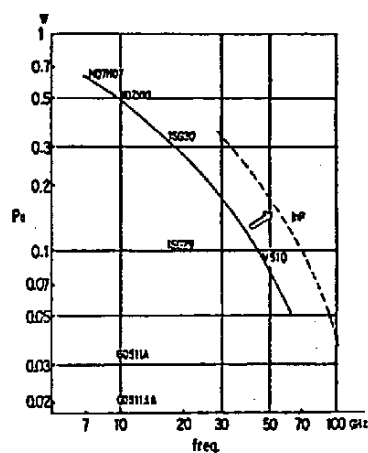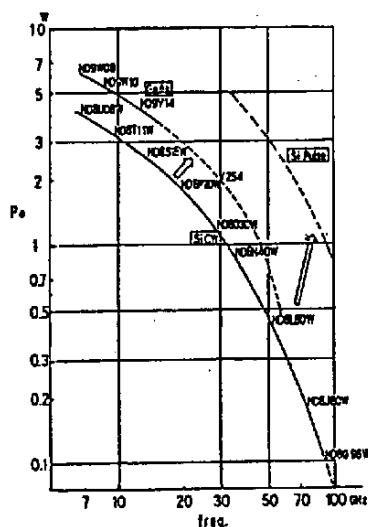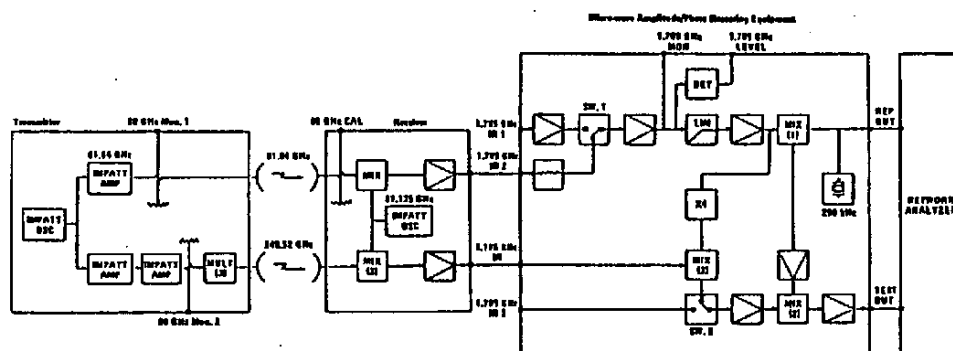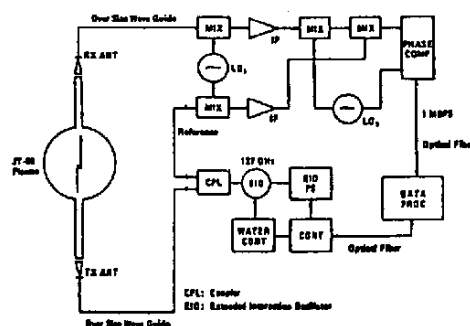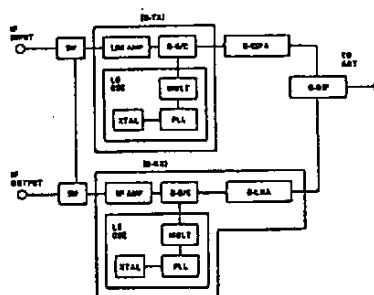
HIGH SPEED OPTICAL DATA LINKS

by

R. Heidemann
Standard Elektrik Lorenz AG, Research Centre
Lorenzstrasse 10, 7000 Stuttgart 40, FRG

1. Introduction

For future broadband networks as B-ISDN or IBCN (Integrated Broadband Com-
munciation Network) very high speed fiber optic transmission systems are
needed. Obviously the application of such systems with multigigabit/s capa-
city will te trunk lines, lines between broadband local exchanges and TV/
HDTV-links for distribution purposes (feeders). But also in the subscriber
area Gbit/s applications will be technically feasible and cost effective,
e.g. very high speed data links and TV/HDTV-links for contribution (inter
and intra studio). Required fiber capacities in the upper Gbit/s range are
very likely to be needed because the bitrate of a digital encoded high qua-
lity colour TV picture and a HDTV picture amounts to 140 Mbit/s and 1 Gbit/s
respectively if no redundancy reduction is applied within the encoder.

Another important application area of Gbit/s transmission is the communica-
tion within and between next generation computers. This high rates would
occur even with todays standard computers if parallel busses (e.g. 70 x 10
Mbit/s) that are running with a low speed per wire are serialized to a more
or less extend.

Today 1.7 Gbit/s fiber-optic trunks are already in service in USA and Japan.
In Germany more than 20.000 fiber kilometers are under operation at

565 Mbit/s. More than 600 line terminations and 1.000 intermediate regenerator have been handed over by German suppliers to the Bundespost. Since July 88 the first 2.24 Gbit/s German Bundespost field trial link supplied by SEL-RC is operational at the FTZ in Berlin. This system runs at 1550 nm over 40 km standard single mode fiber with a bit error rate less than 10^{-15} (no bit error in 3 weeks).

2. Techniques of High Speed Optical Transmission

A major emphasis of today's research in the fiber optics field revolves around comparisons of the performance of IM/DD-type systems against coherent techniques (optical superheterodyne or homodyne receiver, transmitter with frequency or phase shift keying). It is clear that the frequency stabilization (1550 nm = 1.93×10^{14} Hz = 193 000 GHz) of the transmitting laser and the receiver local oscillator laser will be a major problem, because the intermediate frequency (IF) is in the microwave band at several GHz e.g. at 10 GHz which is only a fraction of 5×10^{-5} of the optical carrier frequency. A higher IF (several 100 GHz) is not suitable because the mixing receiver photodiodes are not fast enough and the IF signal processing functions, as amplification and frequency or phase demodulation, are very difficult to realize. As the lasers in the transmitter and receiver are free running oscillators their linewidths are not sufficiently narrow in most cases. Sophisticated and therefore costly stabilization schemes must be used. Nevertheless these problems are unsolved today and are the main contribution to the measured receiver sensitivity degradation of 17 dB (4 Gbit/s, best measured value: -31.1 dBm, quantum limit: -48.5 dBm).

As it looks today coherent systems will be used in the future beneficially for special applications, e.g. submarine links or multichannel systems, provided the problem of laser stabilization to a reference source or to an atomic or molecular resonance line is solved.

Similar wavelength stabilization and tolerance problems are encountered in WDM systems. Today it is not clear in what way the different laser wavelengths of the transmitters can be kept adjusted to the comb-like passbands of the optical filter duplexers. Especially in field environment and over life time this will be a serious problem if densely spaced optical channels (e.g. $\Delta \lambda \sim 5$ nm) are envisaged. For the strategy towards the multigigabit capacity per fiber near to medium future the optimum might be: TDM up to at least 10 Gbit/s, followed by WDM to 40 Gbit/s = 4 x 10 Gbit/s with a moderate channel spacing of 40 nm if required.

From experimental results gained with 1300 and 1550 nm DFB lasers it has been shown that the eye opening of the laser pulse can be increased considerably and that the wavelength chirp can be reduced by more than a factor of two if an appropriately shaped driving current pulse is applied to the laser chip. Using this optimised laser driver and a 1550 nm DFB laser, system measurement at 2.24 Gbit/s and 1550 nm have been performed over a 115 km standard single mode fibre (dispersion zero of 1310 nm) link with the high dispersion of 17 ps/nm x km. The measured bit-error-rate (BER) characteristics show a penalty of 0.5 dB in contrast to the expected value of 7 – 13 dB. The usage of this laser driver leads to an additional bridgeable span length of more than 30 km. Today this driver circuit was realised with GaAs-FETs in distributed microwave circuits on PTFE substrate. In the near future advanced silicon bipolar and GaAs technologies will make the implementation of sophisticated high speed driver chips much easier.

3. High Speed Signal Processing for Optical Transmission Systems

The overall performance of a Gbit/s transmission system, especially of a long haul repeatered link, is to a large extend determined by the performance of the signal regenerator, consisting of decision circuit and clock recovery. Here the noisy and distored signal coming out of the optical receiver is threshold detected and retimed. The amplitude decision ambiguity of the threshold detector must be in the mV-range at the nominal input level

of 1 V_{pp}. The second figure of merit is the clock phase margin which should be well above 250° to avoid a too large penalty due to horizontal eye closure.

At SEL-RC a silicon bipolar decision circuit chip for up to 3 Gbit/s has been developed. An outstanding decision ambiguity of 5 mV_{pp} (nom. input level 1 V_{pp}) and clock phase margin 310° has been measured at the design bit-rate of 2.24 Gbit/s. A complete regenerator chip (decision and clock recovery) is realized at the moment. Recent circuit simulations show that even 10 Gbit/s regenerators, especially the decesion part, could be realized with silicon bipolar. On the other hand GaAs seems to be preferrable for the clock recovery part of the regenerator, if the pll-type is choosen. Detailed simulations based on experimental results (test chips measured in system test beds) will yield the optimum design strategy for the regenerator chips.

The regenerator chip still is a relatively low complexing chip, this situation dramatically changes when multiplexers and demultiplexers are encountered. Here the number of gates sums up to several hundreds to above one thousand depending on the order of multiplexing. As an example low order mux/demux pairs where developed at SEL for 2.6 Gbit/s in silicon bipolar technology. Besides the pure mux/demux function all essential auxilary functions like clock frequency division, clock output driver, frame shift, and bit error rate measurement output were integrated on the chips.

For 10 Gbit/s it is planned to start with a low order mux/demux 4 x 2.4 Gbit/s --> 9.6 Gbit/s to test and compare technologies, e.g. silicon bipolar versus GaAlAs-HBT. In the second step high order mux/demux will be discussed, e.g. 64 x 140 Mbit/sec.

The Future of Gallium Arsenide

K.Shibayama and K.Fujikawa
LSI Research and Devlopment Laboratory
Mitsubishi Electric Corporation
4-1, Mizuhara, Itami, Hyogo 664 Japan

Gallium arsenide material and device technologies have advanced impressively over the past decade. A wide variety of gallium arsenide devices such as field effect transistors, integrated circuits, light emitting diodes, laser diodes, is now widely used in a communication system, a radar system, a broadcasting system, and high speed signal processings. This article overviews the present status, the trends of technologies and applications for gallium arsenide in the future.

1. Technological Trend in GaAs Devices

In this section, the technological trend in GaAs devices will be first described from the material point of view, through two typical examples: GaAs IC as one of high speed electronic devices, and laser diode as one of optical devices. The state-of-the-art on GaAs-on-Si technology (Superhetero epitaxy) will be next described.

1.1 GaAs IC

The technological trend of GaAs ICs is summarized in Table 1. The basic device for building GaAs IC is a field effect transistor (FET) and many FETs are usually fabricated on a semi-insulating GaAs substrate.

An active layer for FET is formed either by ion implantation or epitaxial technology. The ion implantation technology has benefits of flexibility in transistor structure and process simplicity, but at the same time a drawback that the electrical characteristics of the ion implanted layer tend to be influenced by the quality of the underlying semi-insulating GaAs substrate. On the other hand, epitaxial technology offers a benefit of less susceptibility to the substrate quality, but drawbacks in this technology include less flexibility in transistor structure and higher cost due to lower yield in epitaxial process.

For the future penetration of GaAs ICs into the market, it is indispensable to pursue lower cost in addition to higher performance of GaAs ICs. From the cost viewpoint, GaAs IC has a disadvantage that it is fabricated by using an expensive GaAs substrate (GaAs is several tens of times as costly as Si).

In this regard, GaAs-on-Si epitaxial technology is expected to be very important in the future. Making use of this technology, GaAs epitaxial layer is formed directly on a larger sized and less expensive Si substrate by metalorganic chemical vapor deposition (MOCVD).

Wafer size for GaAs IC is, at present, mostly 3" in diameter, although 2" wafers are still partly used. Transition of 3" wafer to 4" is predicted to take place around the middle of 1990s or later when GaAs IC market is expected to show a sharp rise. With respect to the transistor structure, several kinds of new transistors will be used in the future in place of GaAs MESFETs. They are high electron mobility transistors (HEMT) and hetero bipolar transistors (HBT) with hetero junction such as

Table 1. Technological Trend of GaAs IC

		1987	1991	1995
Crystal	Wafer Size	3"φ	3~4"φ	4"φ
	Substrate	undoped/In-doped LEC		
Epitaxial Growth		Hetero epitaxy (AlGaAs/GaAs on GaAs)		Superhetero epi (GaAs on Si)
Process	Gate Length	0.5~0.75μm	0.3~0.5μm	0.1~0.3μm
	σ vth	20mV	10mV	5mV
Transistor Structure		MESFET	SAMFET* HEMT	HBT
Function		single function		multi-function

$*$ Self Aligned Multi-layer gate FET

AlGaAs/GaAs and InGaAs/GaAs and further improvement in the device performance is expected.

In the area of microfabrication technology, the smallest pattern width is now in the range of 0.5 to 0.75μm and is formed mainly by optical lithography such as step-and-repeat system. In the future, finer patterns will be required (for example from 0.3-0.5μm to 0.1-0.3μm) for further improvement of device performance, and the development of electron beam lithography and focused ion beam lithography will become more important.

Functional integration of GaAsIC is also predicted to proceed. For example, single function ICs will be replaced by multi-function ICs in which both analog circuit and digital circuit are integrated.

1.2 Optical Devices

The technological trend of optical devices is shown in Table 2. Semiconductor optical devices are fabricated using hetero epitaxial layers. Liquid phase epitaxy(LPE) has been used to form these layers, but this technology has difficulties in obtaining good surface morphology and a very thin layer with good reproducibility.

In recent years, MOCVD technology has become available to grow high quality epitaxial layers. By this technology, the surface morphology and layer thickness controllability have been significantly improved.

Table 2. Technological Trend of Optical Devices

	1987	1990	1993
Epitaxial Growth	LPE/MO-CVD	MO-CVD	MO-MBE
Device Structure	discrete	discrete,array	OEIC,OIC
Layer Structure	double hetero	quantum well	quantum well wire & box

From the functional point of view, the laser diode will evolve into OEIC where electronic devices and optical devices are integrated , or OIC where several optical devices having different functions are integrated .

—201—

1.3 GaAs-on-Si Epitaxial Technology

It is generally very difficult to grow GaAs epitaxial layer directly on a Si substrate, since physical properties of Si and GaAs, especially crystal structure, lattice constants and thermal expansion coefficients differ from each other.

The difficulties in GaAs-on-Si epitaxy due to these physical property differences are summarized as follows:

i) Difference in crystal structure (Si has a diamond crystal lattice, while GaAs has a zincblende lattice) results in antiphase disorders which are one of the typical crystal defects).

ii) Lattice mismatch (lattice constants for Si and GaAs are 5.43Å and 5.65Å, respectively) and difference in thermal expansion coefficient result in generation of dislocations.

Unless the above difficulties are overcome, dislocations as high as 10^8 to $10^9/cm^2$ will be introduced in the epitaxial layer, and thereby it is impossible to fabricate electronic or optical device in the layer. The above first difficulty is solved by using Si substrate oriented 2 off the (100) plane towards $< 110 >$. The second difficulty was considerably overcome by introducing cyclic-thermal-annealed buffer layer and strained layer superlattice structure between GaAs epitaxial layer and Si substrate, and the resulting dislocation density is reduced to as low as $10^6/cm^2$.

Solar cell was fabricated using this GaAs-on-Si wafer and the effective conversion efficiency of 16.8% for $1cm \times 1cm$ cell was realized. This efficiency is very close to 18 – 19% for GaAs on GaAs solar cells now in the production stage. This result suggests the potentiality of the GaAs-on-Si epitaxial technology to be applied to the fabrication of various devices, such as FET , GaAs IC, laser diode and OEIC, accompanied by lowering the dislocation densities.

2. Application Trend

2.1 Electronic Devices

Figure 1 shows the application trends of GaAs electronic devices. GaAs FETs, AlGaAs/GaAs HEMTs and GaAs analog ICs are widely used as amplifiers and oscillators for the radar system, the satellite broadcasting system, the mobile communication system, instrument, etc. Further improvement of these devices aiming at lower noise, higher frequency and lower cost will continue, and will accelerate the enlargement of application area and market volume.

In digital applications, on the other hand, GaAs ICs now in use remain in the level of SSI and MSI, like standard logic and prescaler for instrument and automobile telephone systems. As described before, together with further improvements in semi-insulating crystal quality, hetero-epitaxial technology, and microfabrication technology, GaAs memory and logic LSIs superior to Si counterpart will be available and be applied to the very high speed signal processor for the radars, the supercomputer, the instrument, etc. Probably it will not be until the middle of 1990s that such time will come.
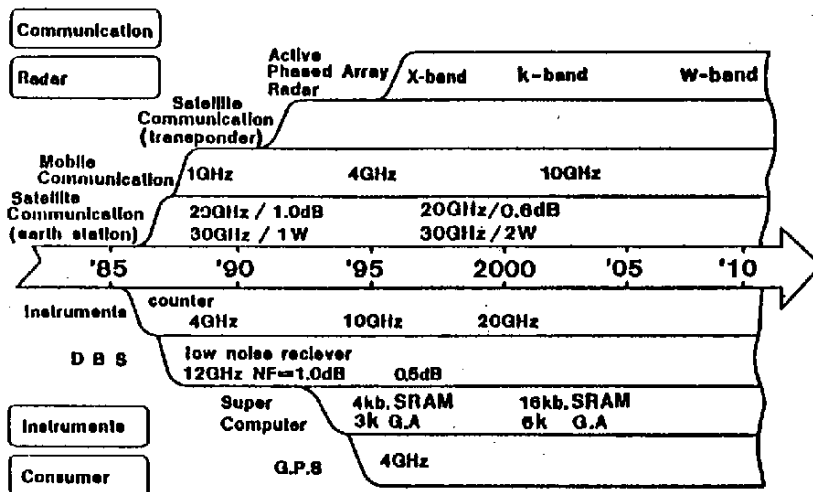
Figure 3. Application of GaAs electronic devices

2.2 Optical Devices

Figure 2 shows the application trends for optical devices such as LEDs and laser diodes. Major application area of semiconductor lasers are as follows:

(i) Optical communication system, such as for trunk line, subscriber loop, and local area network (LAN)

(ii) Information processing system, such as laser printers, optical disc memories, bar code readers, laser cards

(iii) Home electronics system, such as compact discs, and video discs

(iv) Optical instrument, such as levelers, and transits

In the future, through the developments of single mode lasers, OEIC, OIC, etc., it will not be just a dream to realize optical computers around the turn of the century that can process a vast amount of information at very high speed.
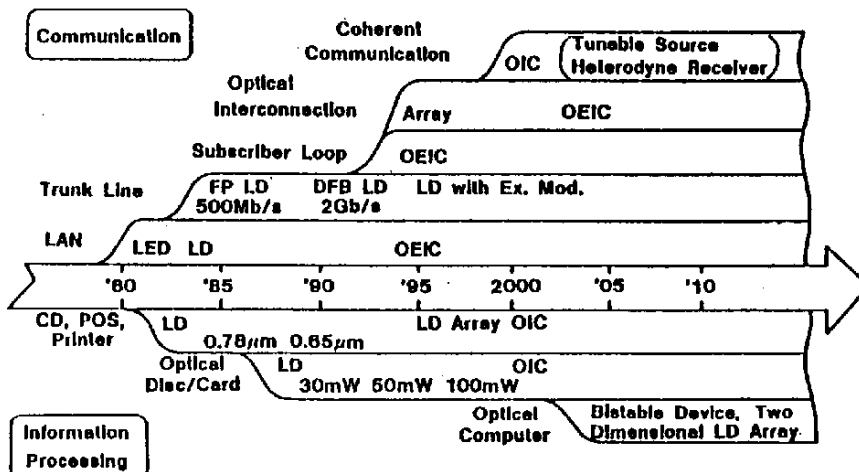
Figure 4. Application of optical devices

Features of GaAs Devices
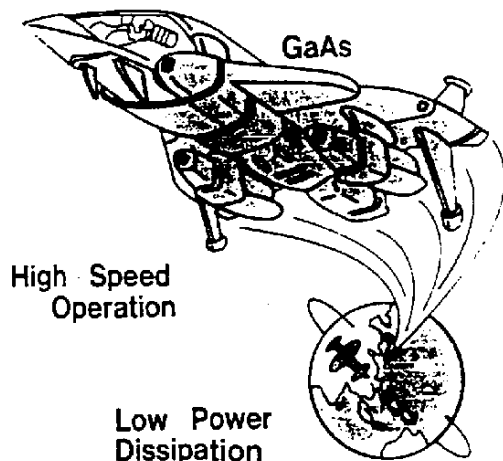
GaAs
High Speed Operation
Low Power Dissipation
GaAs
Si
Light Emitting Properfies
Excellent Radiation Hardnes
GaAs
200°C
Si
MITSUBISHI ELECTRIC CORPORATION
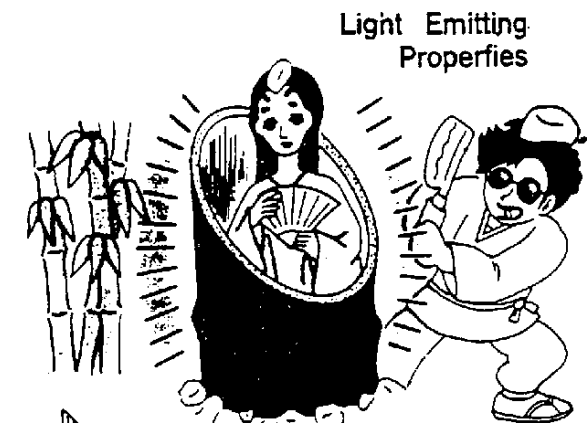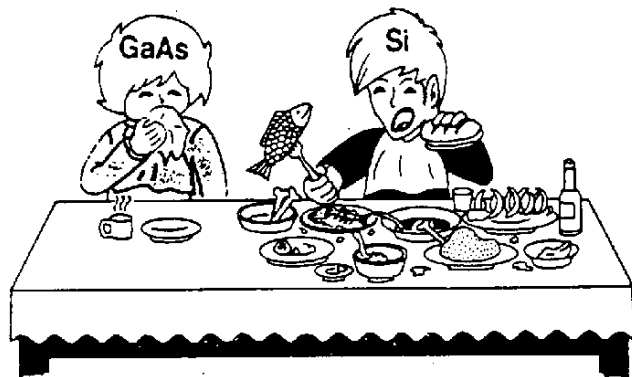
G.P.S.

business
communication.

satellite
communication

Communication

automobile telephone
communication

F.C.S.
for ship or fighter

phased array radar

Defense

E.C.M.

millimeter wave
seeker

GaAs IC

super
computer

instrument

Consumer

rescue
system

DBS

APPLICATION OF SEMICONDUCSOR LASER & RELATED DEVICES
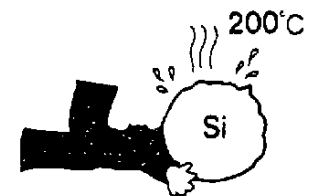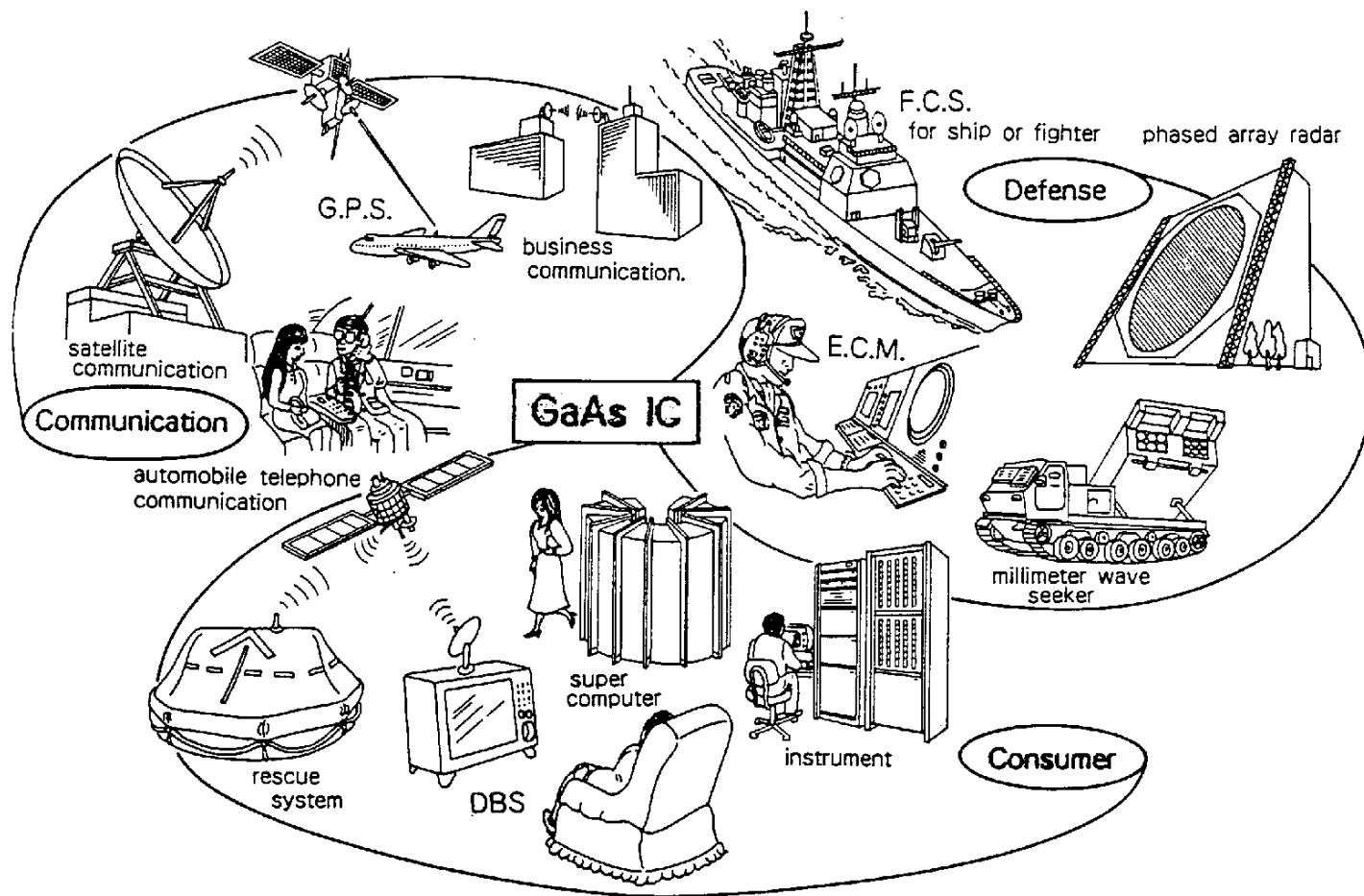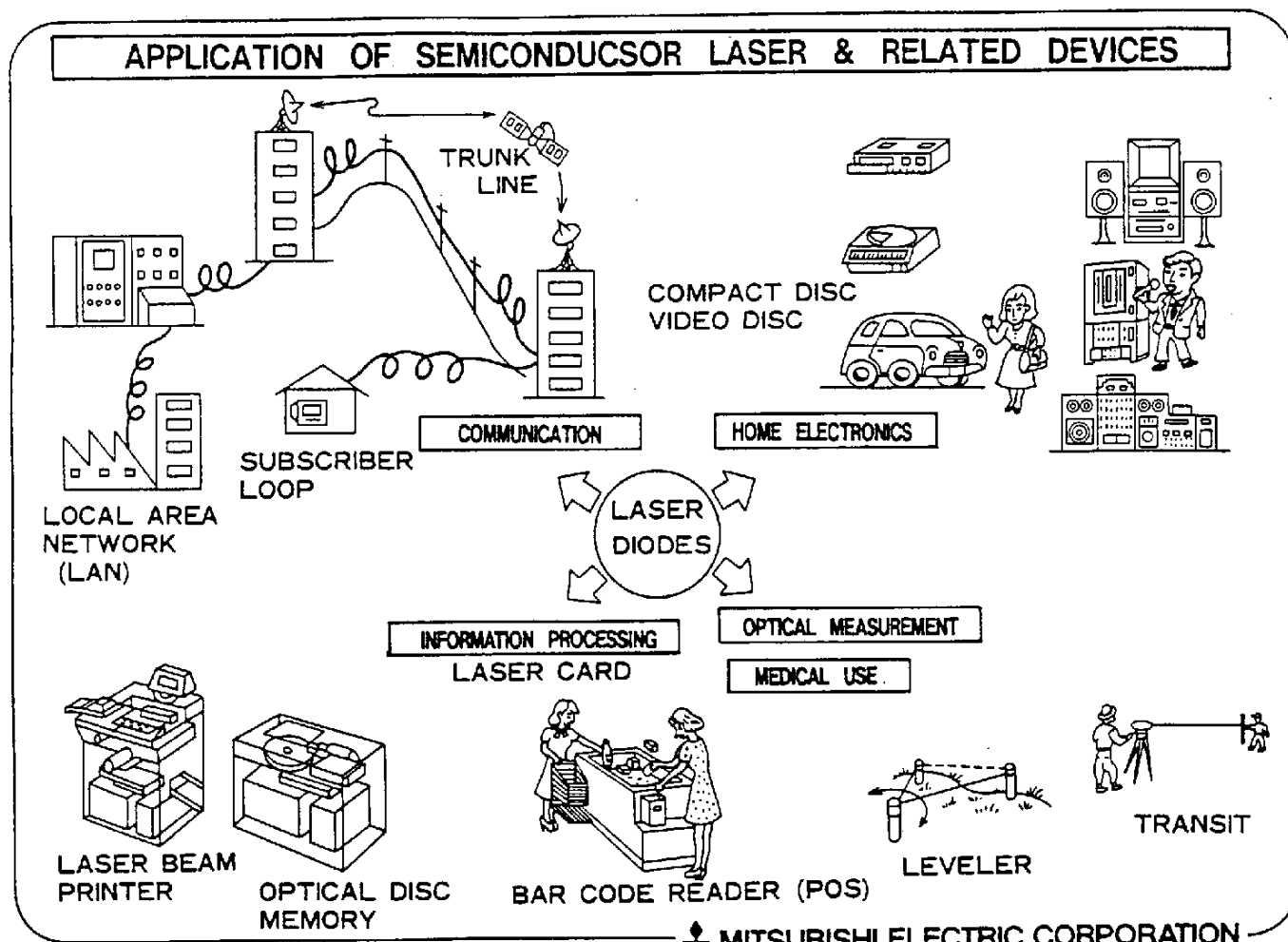
Technological Trends of GaAs ICs

		1987	1991	1995
Crystal	Wafer Size	3"ϕ	3~4"ϕ	4"ϕ
	Substrate	undoped/In-doped LEC		
Epitaxial Growth		Hetero epitaxy (AlGaAs/GaAs on GaAs)		Superhetero epi (GaAs on Si)
Process	Gate Length	0.5~0.75μm	0.3~0.5μm	0.1~0.3μm
	σ Vth	20mV	10mV	5mV
Transistor Structure		MESFET	SAMFET HEMT	HBT
Function		single function		multi-function

* ref.[1]

Trend of the Delay Time for Several Types of Memories

(4Kb Memory)

MESFET

MESFET

HEMT

HBT/SIS

Improved Uniformity
(σVth≦3∼5mV)
Improved Crystal
Quality
Shortened Gate Length
(Lg≦0.5∼0.7μm)
Reduced Short Channel
Effect

Reduced Surface Defects
Abrupt Hetero Epitarial
Interface
Improved Thickness Uniformity

Delay Time(ns)

10

5

1

1985   1990   1995   2000

Year
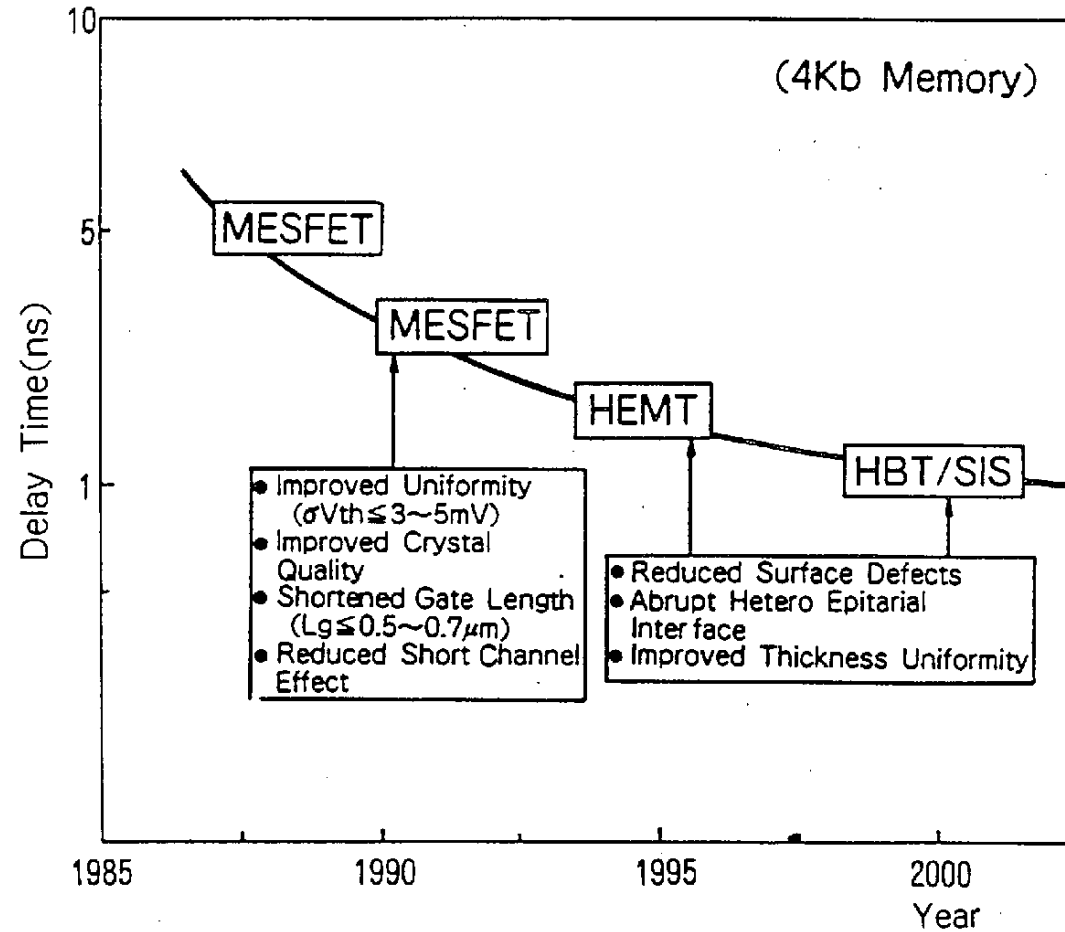
Technological Trends of Optoelectronic Devices

	1987	1990	1993
Epitaxial Growth	LPE/MO-CVD	MO-CVD	MO-MBE
Device Structure	discrete	discrete,array	OEIC,OIC
Layer Structure	double hetero	quantum well	quantum well wire & box

▲MITSUBISHI ELECTRIC CORPORATION

GaAs-on-Si Super-Hetero Epitaxial Technology

GaAs

Si

5.65Å

Dislocation

5.43Å
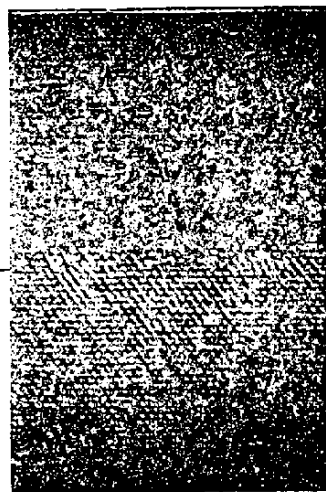
A Cross-sectional TEM Image for the GaAs/Si Interface
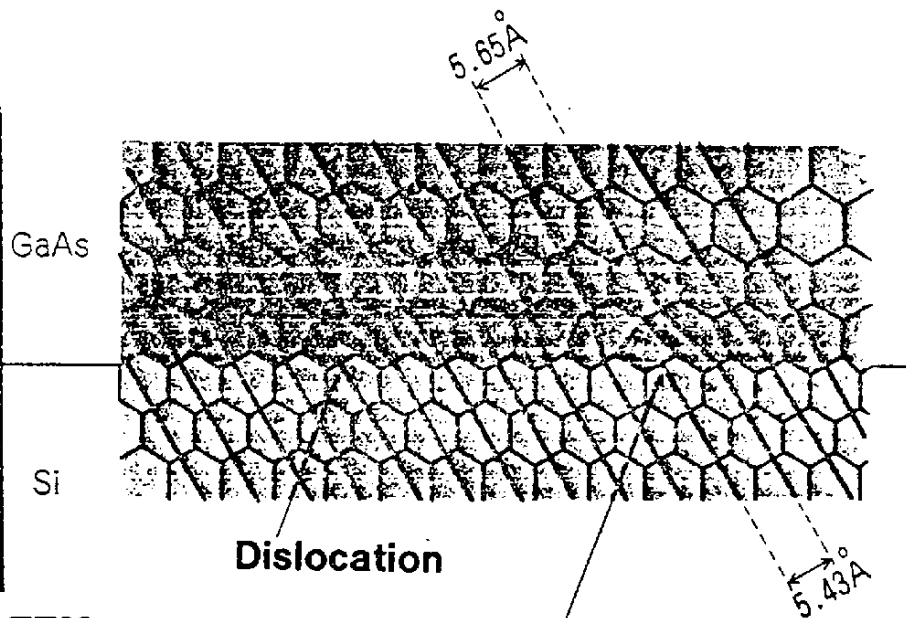
A Schematic Drawing of the GaAs/Si Epitaxial Interface

MITSUBISHI ELECTRIC CORPORATION

GaAs on Si Epitaxial Technology

Lattice Matched Buffer Layer
- cyclic thermal annealing
- strained superlattice

GaAs

dislocation
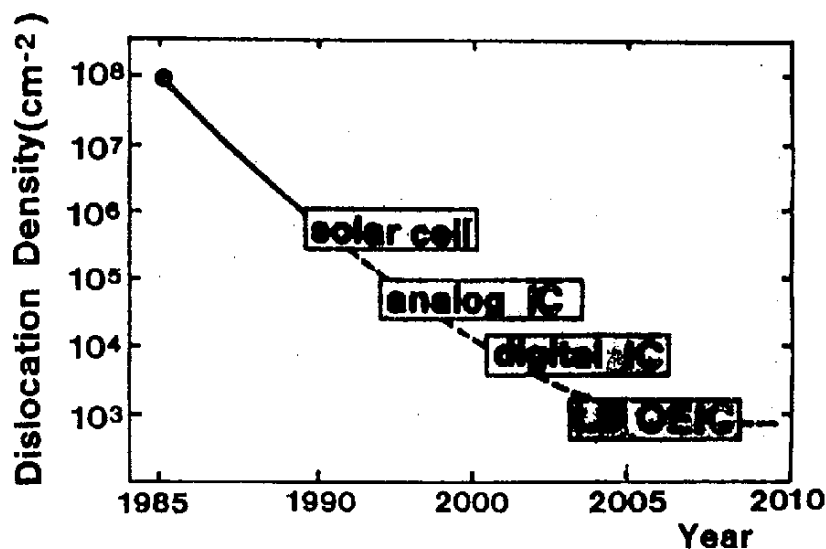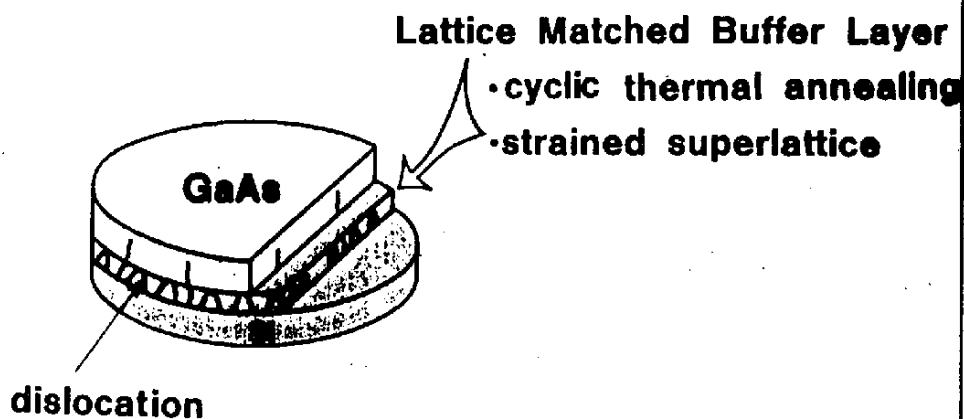
MITSUBISHI ELECTRIC CORPORATION

Application Trends of the GaAs ICs

Communication

Radar

Active Phased Array Radar	**X-band**	**k-band**	**w-band**

Satellite Communication (transponder)

Mobile Communication — 1GHz   4GHz   10GHz

Satellite Communication (earth station) — 20GHz / 1.0dB   20GHz/0.6dB
30GHz / 1 W   30GHz /2W

'85   '90   '95   2000   '05   '10

Instruments — counter   4GHz   10GHz   20GHz

D B S — low noise reciever   12GHz NF=1.0dB   0.5dB

Instruments — Super Computer   4kb.SRAM   16kb.SRAM
3k G.A   6k   G.A

Consumer — G.P.S   4GHz

MITSUBISHI ELECTRIC CORPORATION

—212—

Multi-Functional GaAs IC
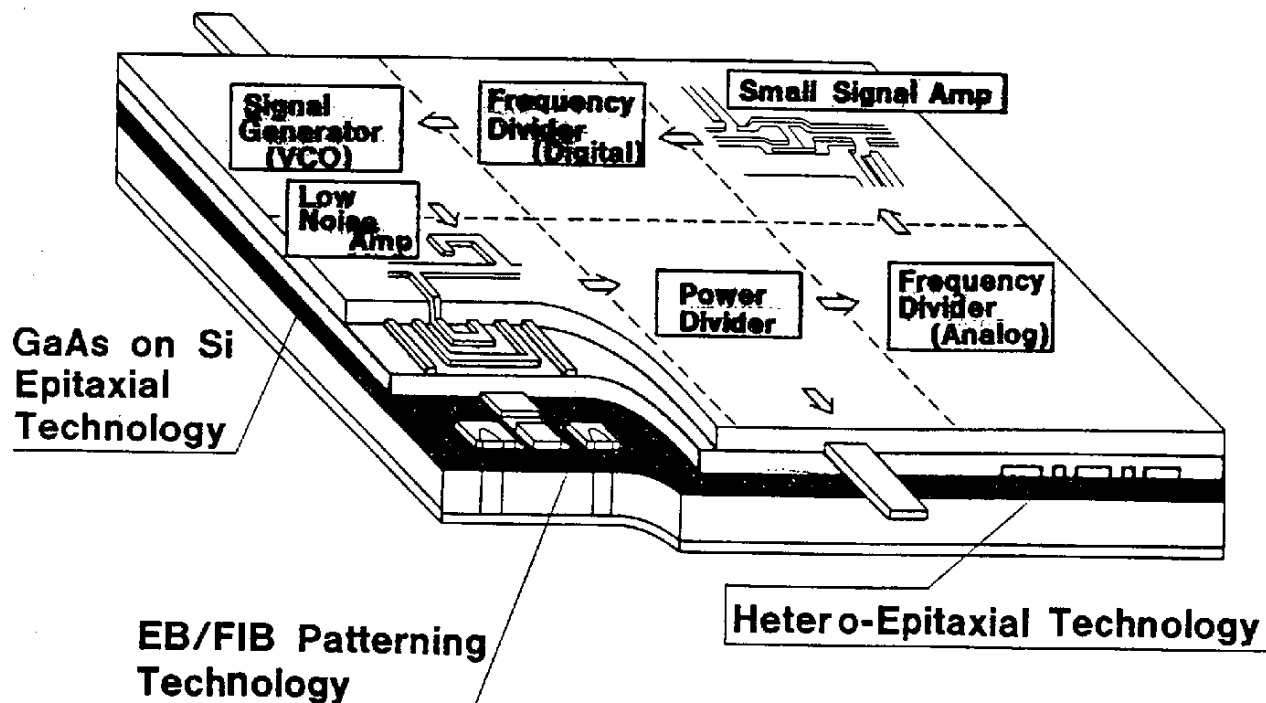
Application Trends of Optoelectronic Devices

Communication

Coherent Communication

Optical Interconnection

Subscriber Loop

Trunk Line — FP LD 500Mb/s   DFB LD 2Gb/s   LD with Ex. Mod.

LAN — LED LD   OEIC

OIC   Tunable Source / Heterodyne Receiver

Array   OEIC

OEIC

'80   '85   '90   '95   2000   '05   '10

CD, POS, Printer — LD   0.78μm 0.65μm   LD Array OIC

Optical Disc/Card — LD   30mW 50mW 100mW   OIC

Optical Computer   Bistable Device, Two Dimensional LD Array

Information Processing

MITSUBISHI ELECTRIC CORPORATION

OEICs

Transistor

Laser

Driver

Substrate

Photo Detecter

The Role of GaAs in Future Information Systems

by Karl Platzöder

1. Introduction

SIEMENS is engaged in GaAs electronics since many years but still
we don't know a simple answer to how important this technology
will be for future information systems.

Based on our own experience with this topic, that proved to be
very interesting for technologists but rather difficult for
marketing people, a guess is made about the trends in the next
future.

2. Materials

The starting material for ion implanted digital and microwave
integrated circuits usually is semi-insulating GaAs.

SIEMENS, besides its own material activities, has close contacts
with external material suppliers to share experience.

Some results about the homogeneity of doping profiles and the
uniformity of threshold voltages is presented out of our work on
digital circuits.

For optimized microwave performance the GaAs background doping
has to be modified. Examples of the type of improvements obtained
this way are given.

The highest performance devices, however, use epitaxial layers.
If methods like MBE and MOCVD become less expensive and more
reproducible, we see their importance growing in all fields of
GaAs electronics.

3. Digital circuits

There have been strong efforts in the last few years to develop a substancial market for digital devices based on ion implantation in semi-insulating material.

SIEMENS too has experimented with circuits like:

o   ⋮Multiplexer and Demultiplexer

o   Prescaler

o   ECL - replacements

o   S - RAM.

To illustrate the situation, some results are presented.

They were incouraging in the beginning, but in the meantime the big improvements in fast silicon bipolar circuits have reduced the market chances for this generation of GaAs devices.
Work now is concentrating on more advanced selfaligned technologies and heterobipolar structures. Circuits to be explored next are fast A/D converters.

4. Microwave circuits

The oldest and still most important application of GaAs (besides optical applications) is in microwaves.
The basic components to be considered are:

o   MESFET's and HEMT's

o   low noise receivers

o   amplifiers

o   switches

o   high power amplifiers

Examples of such components SIEMENS has developed will be presented.
The major interest is in front-end devices for satellite reception, radio links and mobile communication, were we see the main applications for GaAs technologies in the foreseeable future.

It should be noted, however, that military applications like fully phased array radars, mainly in the USA and to a lesser extent also in Europe, are at least as strong technology drivers as the civilian applications mentioned above.

Karl Platzöder is head of the small signal transistor and gallium arsenide IC business group in the SIEMENS semiconductor division.
He joined SIEMENS in 1969 working first on high power thyristors and diodes.
Since 1983 he has been responsible for product development of discrete small signal components and for microwave GaAs - IC's.
In 1988 he became head of this business group.
Dr.Platzöder holds a PhD in physics from the university of Munich.

HEMT AND RELATED NEW DEVICES TECHNOLOGY: STATUS, TREND AND POSSIBLE IMPACT ON FUTURE HIGH SPEED SYSTEMS

Koichi Dazai

FUJITSU LABORATORIES LTD.

10-1 Morinosato-Wakamiya, Atsugi 243-01, Japan

1 INTRODUCTION

Information processing in the 1990's will require ultrahigh-speed computers, with high-speed circuitry with logic delays less than a hundred picoseconds. Toward this end Si devices have been getting smaller and smaller. Despite our advanced technology, we question how long we can continue without basing devices on new physical principles. The research and development of HEMTs and other devices offer solutions.

The HEMT developed by Fujitsu in 1980 was welcomed for use in super-low noise devices and ultrahigh-speed LSI's. In 1981, a HEMT ring oscillator with a gate length of 1.7 μm exhibited a 17.1 ps switching delay with 0.96 mW power dissipation per gate at 77K. This suggests that the HEMT will be used in high speed and low power LSI circuits.

In 1984, the HEMT 1K bit static RAM was developed, and HEMT LSI development began. New high-speed devices, such as the heterojunction bipolar transistor (HBT) were developed in 1985.

2 HEMT

2.1 Low Noise HEMT

Figure 1 compares the low noise performance of 0.5 μm gate-HEMTs and commercial MESFETs. The optimum noise figure and the associated gain at room temperature are 1.1 dB and 10 dB at 12 GHz. At 20 GHz they are 1.8 dB and 8 dB.

This is the lowest noise figure yet reported. The low noise HEMT is already employed in the direct broadcasting satellite (DBS) systems and in radio astronomy amplifiers.

2.2 HEMT LSIs

Figure 2 compares the IC complexity of Si, GaAs MESFET, and HEMT memory. Advances in HEMT memory have been very rapid; fourfold every year. This is mainly because Si techniques now used are compatible with HEMT LSI techniques. Furthermore, HEMT devices are very flexible (Fig. 3).

A thin AlGaAs layer to act as a stopper against selective dry etching is embedded in the top GaAs layer when E- and D-HEMTs are fabricated on the same wafer. The unique epistructure associated with this selective dry etching technique is a key factor for making E/D-FET logic with precisely controlled threshold voltage. Uniformity of threshold voltage is measured for E- and D-HEMTs over the entire 2-inch diameter wafer. The standard deviation of threshold voltage was 24 mV for D-HEMTs and 16 mV for E-HEMTs. These results indicate threshold voltage control more than adequate enough for use in LSI circuits.

A HEMT 16K bit static RAM, with a minimum address access time of 3.4 ns at 77K, at a supply voltage of 1 V has been fabricated. The power dissipation was 1.3 W (Fig. 3).

The 4.1K gate array consists of 156 I/O cells and 4096 basic cells (Fig. 4). Basic gate delay time was 40 ps, and propagation delay time at of FI/FO=3/3, and a wiring-length of 1 mm, was 95 ps. The multiplication time of 16x16 bit parallel multiplier was 4.1 ns with chip power consumption of 6.2 W at 300K.

Present research on HEMT LSIs is part of the National Research and Development Program on the "Scientific Computing System," conducted under the Agency of Ondustrical Science and Technology, Ministry of International Trade and Industry of Japan.

3 NEW DEVICES

3.1 HBT

HBT is the fastest device in the semiconductor device field at 2.6 ps with a power consumption of 60 mW/gate. This performance was achieved by improving the thin base layer and graded collector layer to decrease the intervalley Γ-L scattering. HBT will be used in the MSI circuits because of their high power consumption (Fig. 5).

3.2 RHET

In the future, wiring delay is expected to become a serious problem for VLSI. RHETs are expected to perform new functions and enable a large reduction in the number of components in integrated circuits. This will reduce wiring delays. For example, an Exclusive-NOR gate can be built with only one RHET and resistors (Fig. 6).

The RHET was developed under the direction of the R and D Association for Future Electron Devices as a part of the R and D Project of Basic Technology for Future Industries sponsored by the Agency of Industrial Science and Technology (MITI) of Japan.

4 CONCLUSION

Low noise HEMT's are already used in satellite communications and radio astronomy. A 16K bit HEMT static RAM and a 4.1K HEMT gate array with a 16 x 16 bit parallel multiplier was shown. HBTs have excellent high-speed performance. RHETs offer new functions and are promising for large-scale and high-density integrated circuits.
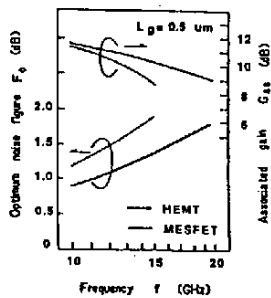
Fig. 1 Low Noise performance of
0.5 μm gate-HEMTs and MESFETs.
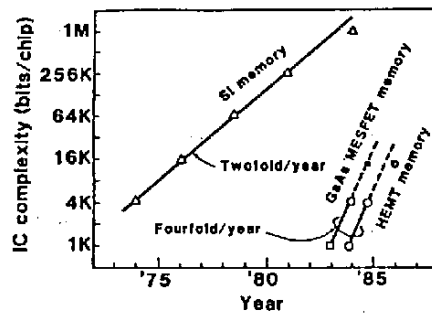
Fig. 2 Advance in the IC complexity
of Si, GaAs MESFET and HEMT memory.
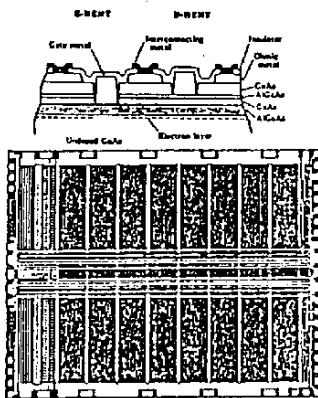
Fig. 3 Crosssection of the self-
aligned structure of E/D-HEMT
forming an inverter for DCFL
circuit (upper) and micro-
photograph of 16K static RAM
(lower).
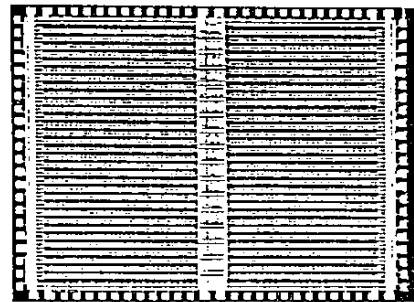
Fig. 4 Microphotograph of 4.1K
gate array.
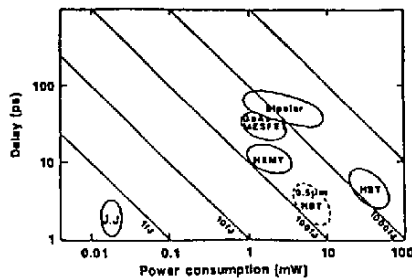
Fig. 5 Comparison of power-delay
relation between bipolar, GaAs
MESFET, HEMT and HBT.
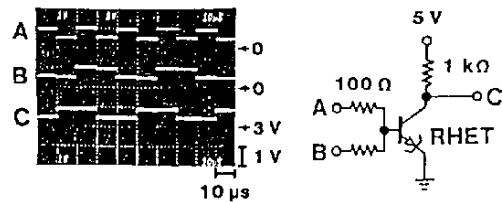
Fig. 6 Exclusive-NOR logic application
using a RHET.

HEMT AND RELATED NEW DEVICES TECHNOLOGY:
STATUS, TREND AND POSSIBLE IMPACT
ON FUTURE HIGH SPEED SYSTEMS

Koichi Dazai

FUJITSU LABORATORIES LTD.

10-1 Morinosato-Wakamiya, Atsugi 243-01, Japan

Outline

1. Why   HEMT ?

2. Advances in low noise HEMT and HEMT
   LSI

3. Advances in HBT and RHET

Application	Device requirements	HEMT performance
Digital:		
SSI/MSI	High average f_T over the ΔV_L	High μ and νs values at 300 K and
LSI/VLSI	Highly uniform threshold voltages High g_m at a small ΔV_L Simple structure	σV_{TH} = 16 mV over 2″ dia wafer (77 K) = 650 mA/V^2·mm L_G = 6 masks for 2-level interconnectio
Analog:		
Low noise	High f_T at low drain currents	f_T = 30 GHz I_{DS} = 5 mA W_G/L_G = 200/0.5 μm
MMIC	High f_T] max High f_{max} Highly uniform device parameters Stable characteristics	f_T] max = 38 GHz L_G = 0.5 μm f_{max} = 65 GHz L_G = 0.5 μm $\sigma g_m/g_m$ = 1.5% over 2″ dia wafer no short channel effect
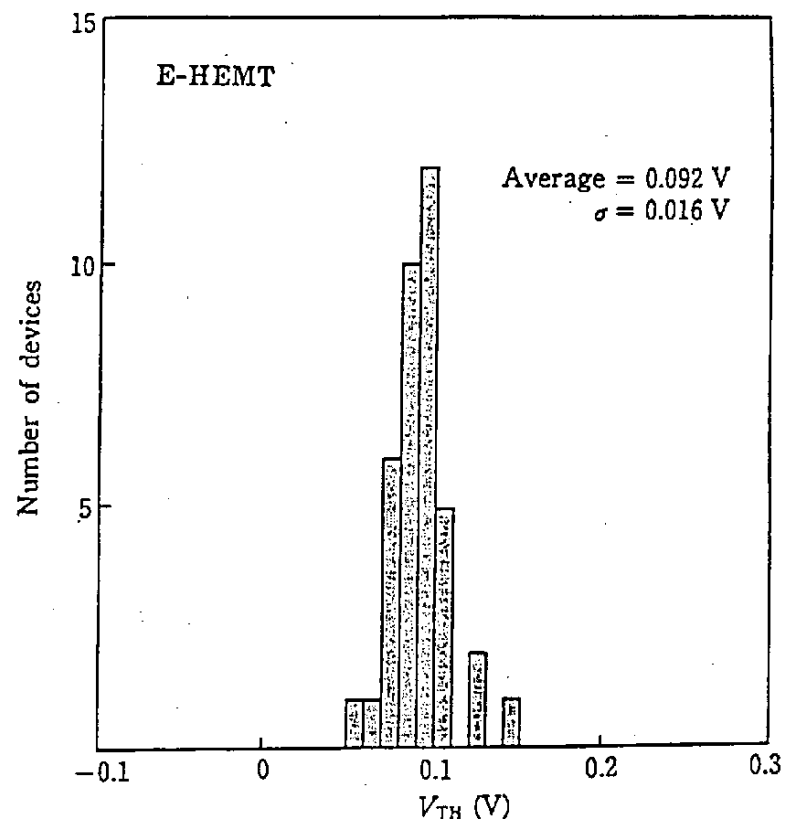
Long range uniformity (2 inch full wafer)
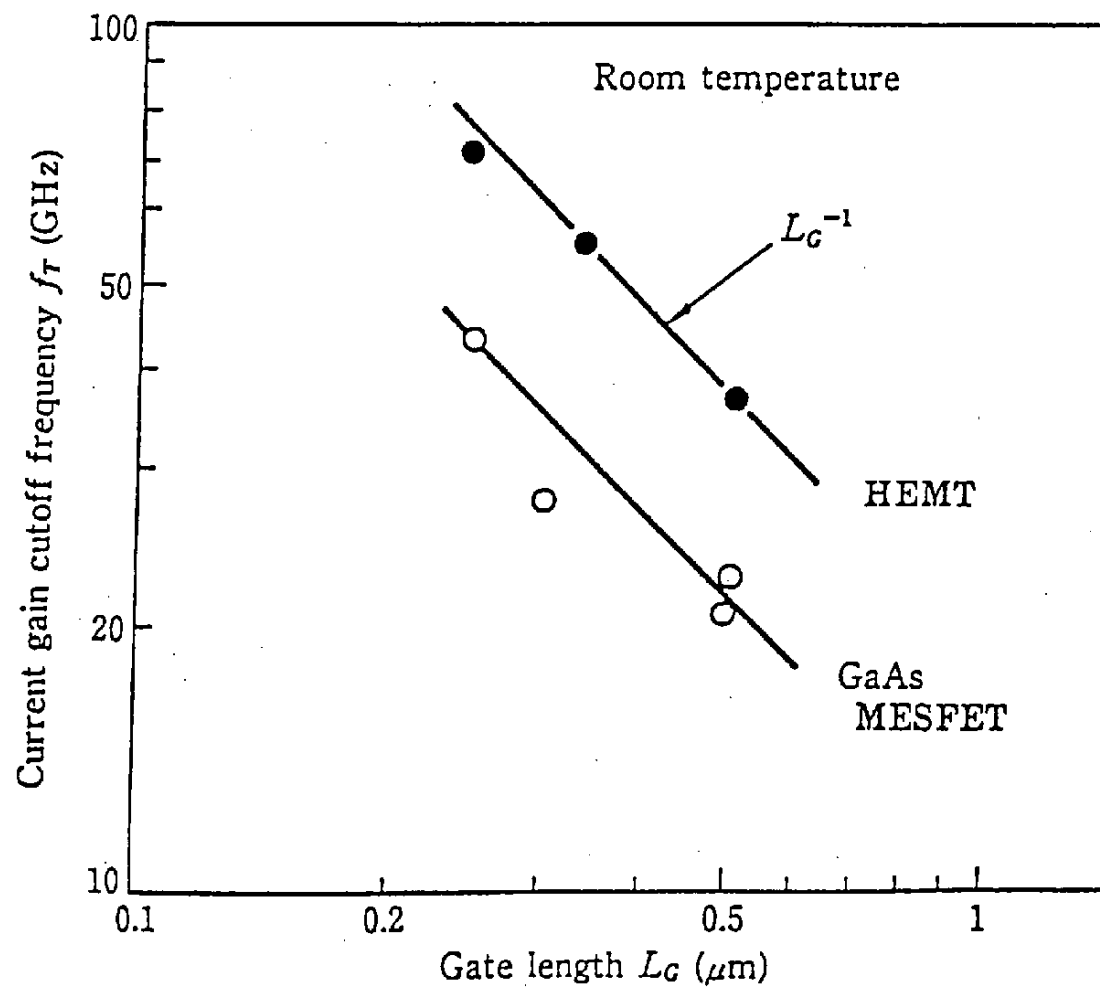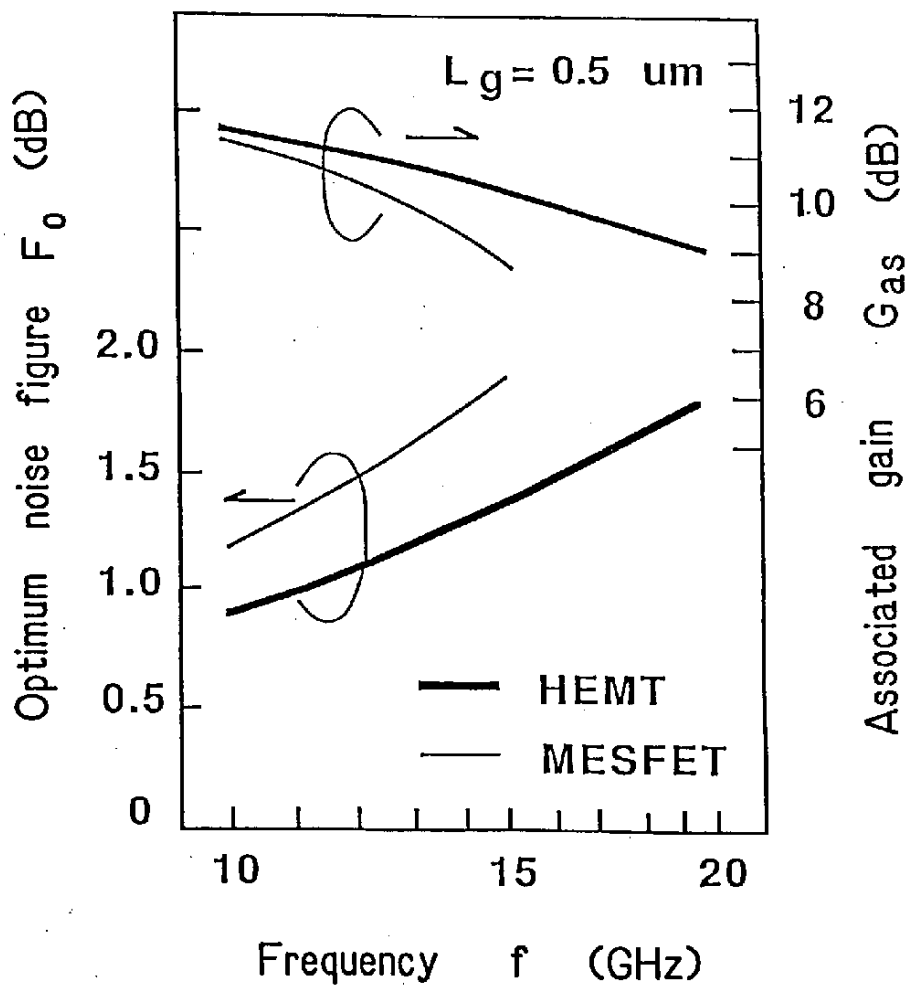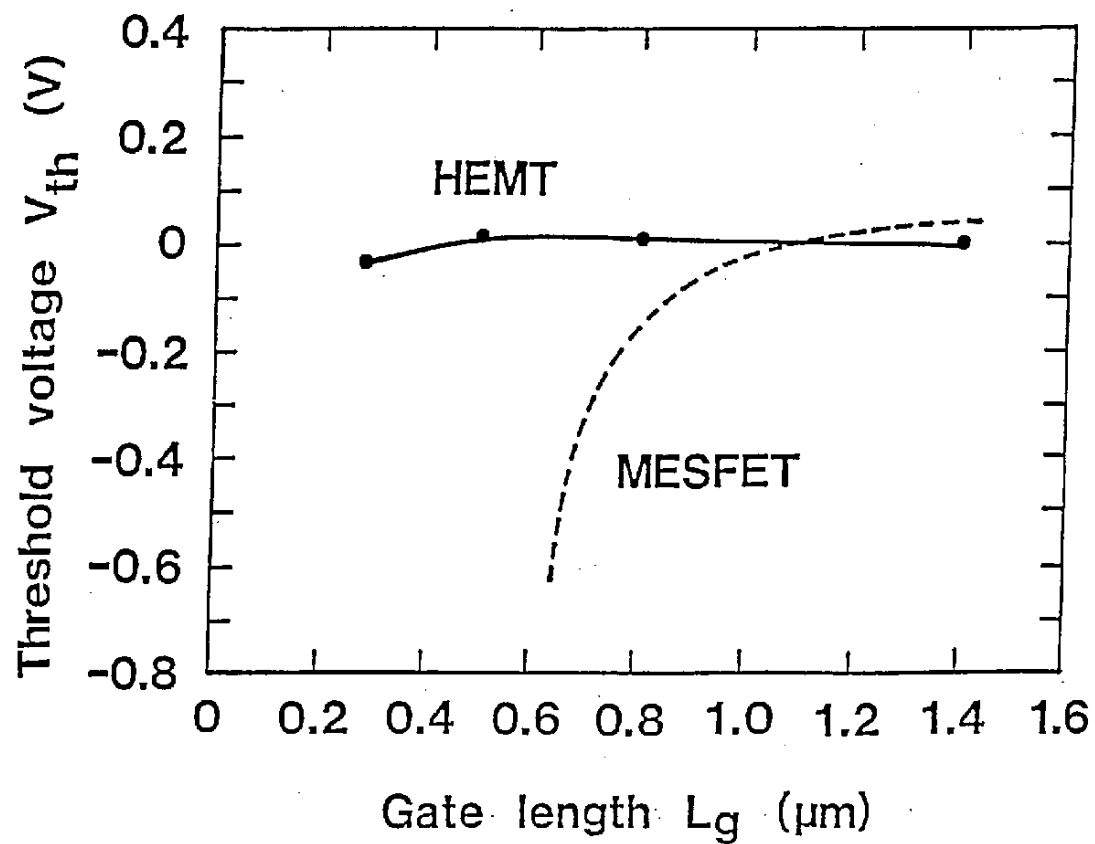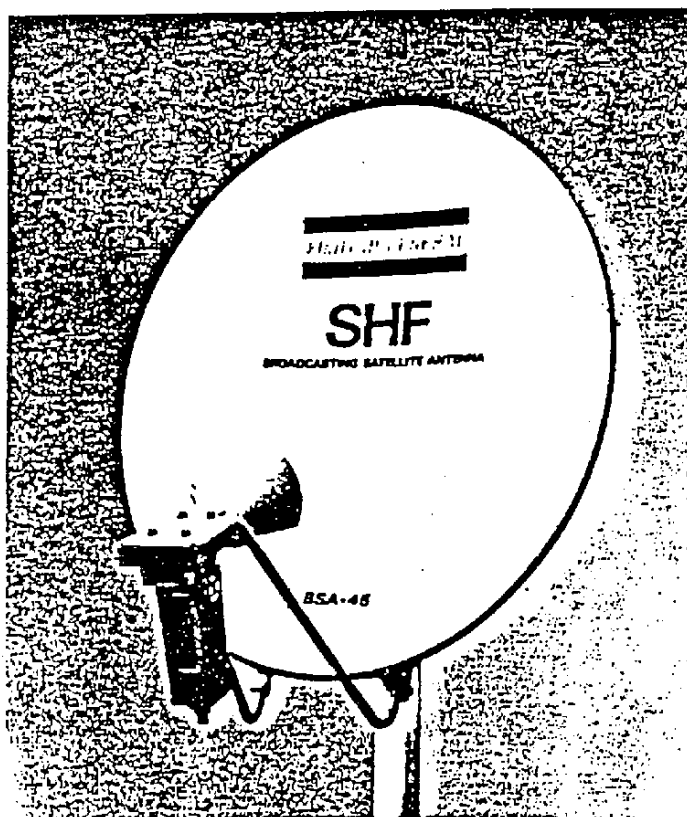
Paraboric antenna for the receiver of the BS system
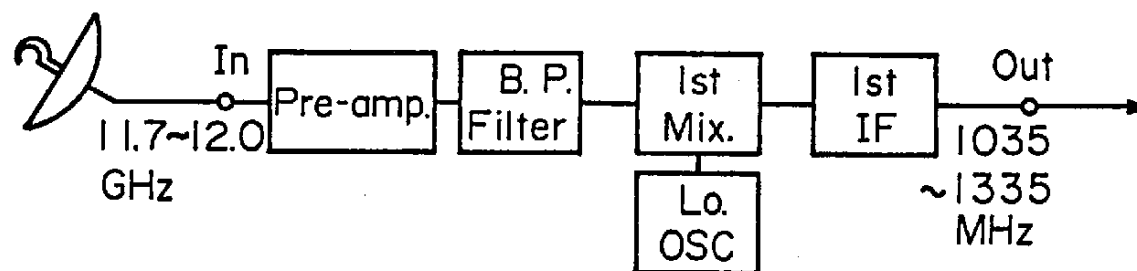
(a)
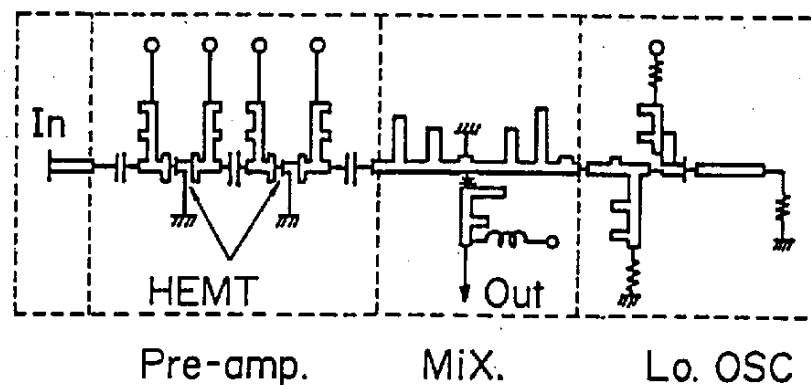
(b)

Block diagram and MIC pattern of BS converter
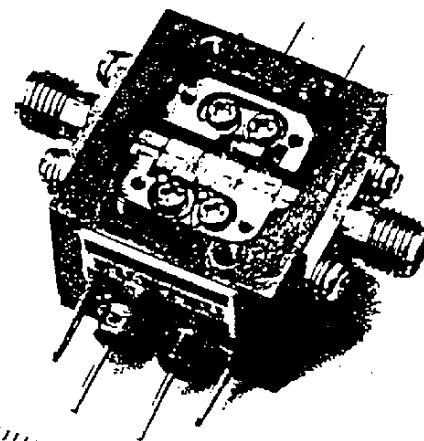
Two-stage HEMT amplifier

E-HEMT   D-HEMT
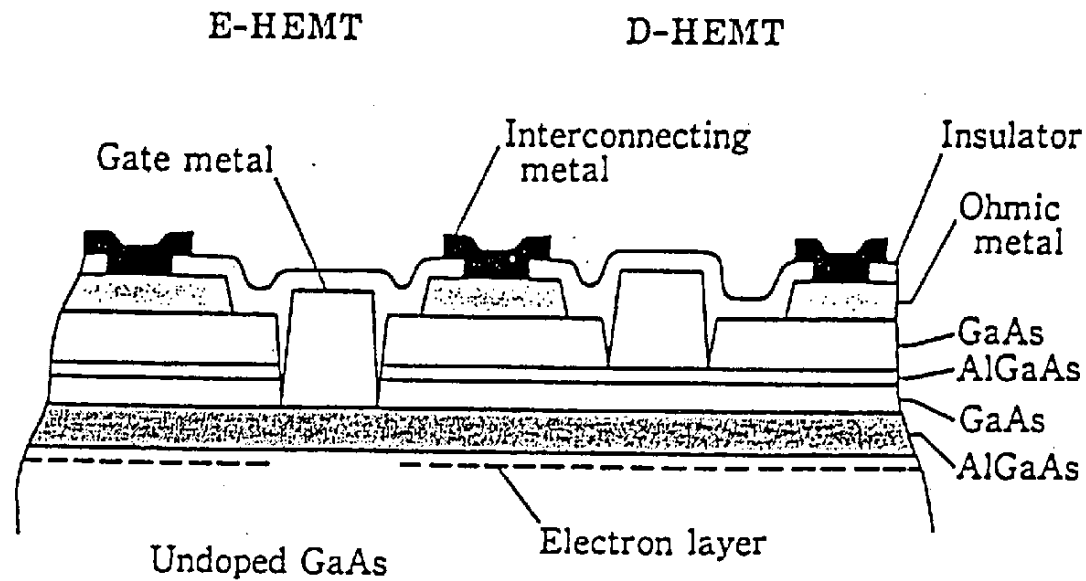
Cross section of enhancement/depletion mode inverter for HEMT direct-coupled FET logic circuit.
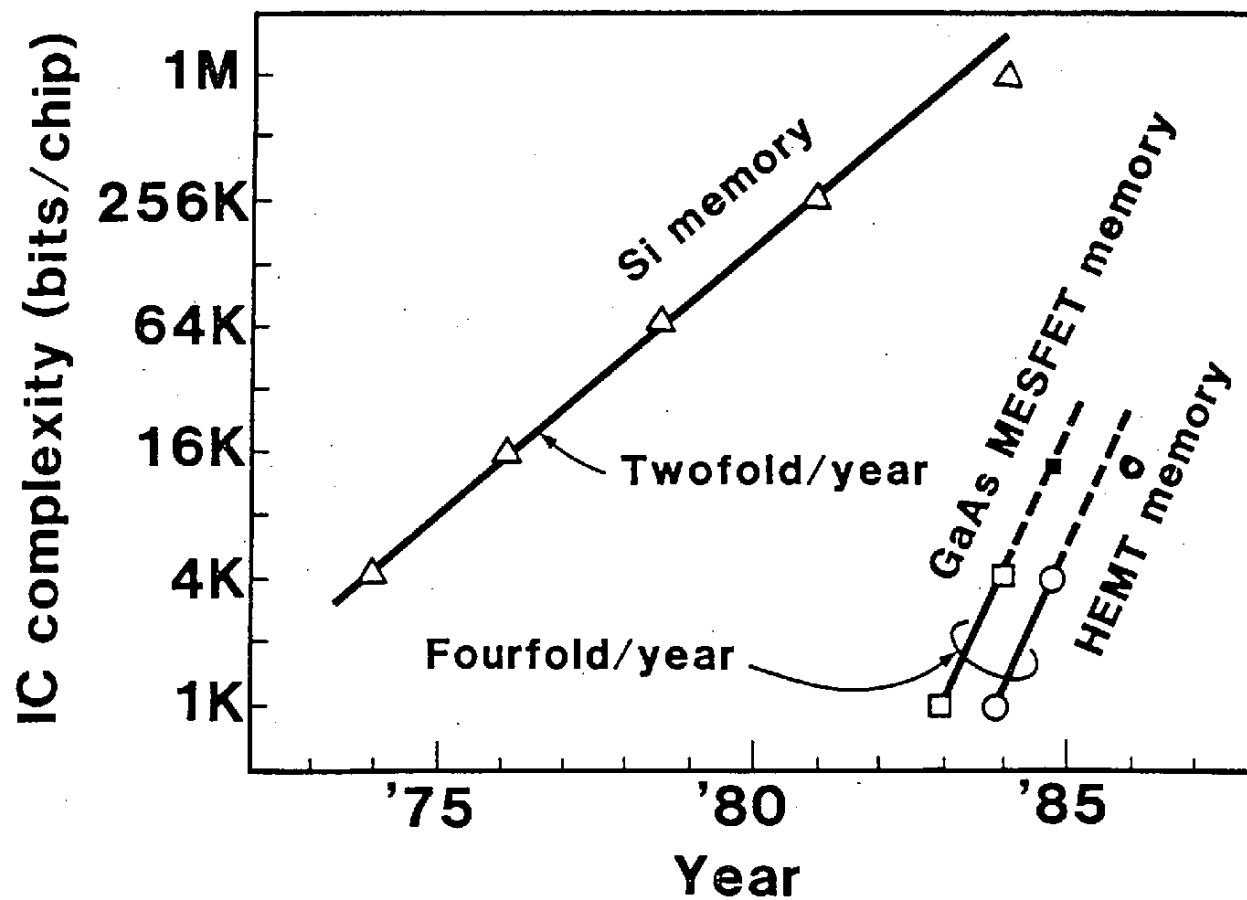
Advances in complexity of HEMT LSI : memory

Source	Function	Complexity (gate)	Performances			Chip size (mm)	Technology	Year
			Delay time (ns)	Power (W)	Temperature (K)			
Fujitsu	Gate array (8 x 8 Multiplier)	1520	3.1	3.2	77	5.5 x 5.6	E/D DCFL L_G = 1.2 µm	1986
	Gate array (16 x 16 Multiplier)	4096	4.1	6.2	300	6.3 x 4.8	E/D DCFL L_G = 0.8 µm	1987
	Data register	1137	0.49	4.1	300	6.1 x 6.2	E/D DCFL, ECL Interface L_G = 0.5 µm	1988
Oki	Gate array (6 x 6 Multiplier)	1000	5.0	0.977	77	3.8 x 4.2	SBFL, Inverted Structure L_G = 0.8 µm.	1987
AT & T Bell Lab.	4 x 4 Multiplier	141	1.6	0.053	300	1.1 x 1.2	DCFL, L_G = 1.0 µm	1985
Honeywell	5 x 5 Multiplier	350	1.08	0.75	77	1.86 x 1.54	DCFL, L_G = 1.0 µm	1986
	8 x 8 Multiplier	1350	3.2	1.9	300	2.7 x 3.9	DCFL, L_G = 1.0 µm	1987
Rockwell	A/D converter D/A converter	(1500 devices)	(140 Mega Sample/s)	—	300	—	L_G = 1.0 µm	1985

Advances in complexity of HEMT LSI : logic

Source	Function	Complexity (gate)	Performances			Chip size (mm)	Technology	Year
			Delay time (ns)	Power (W)	Temperature (K)			
Fujitsu	SRAM	1 K	0.87	0.36	77	3.0 x 2.9	E/D DCFL L_G = 2.0 μm	1984
	SRAM	4 K	2.1	1.6	77	4.76 x 4.35	E/D DCFL L_G = 2.0 μm	1984
	SRAM	16 K	3.4	1.3	77	4.3 x 5.5	E/D DCFL L_G = 1.2 μm	1987
	SRAM	4 K	0.5	5.7	300	2.8 x 3.0	E/D DCFL, ECL Interface L_G = 0.5 μm	1987
Rockwell	SRAM	1 K	0.6	0.45	300	2.5 x 2.35	E/D DCFL L_G = 1.0 μm	1986
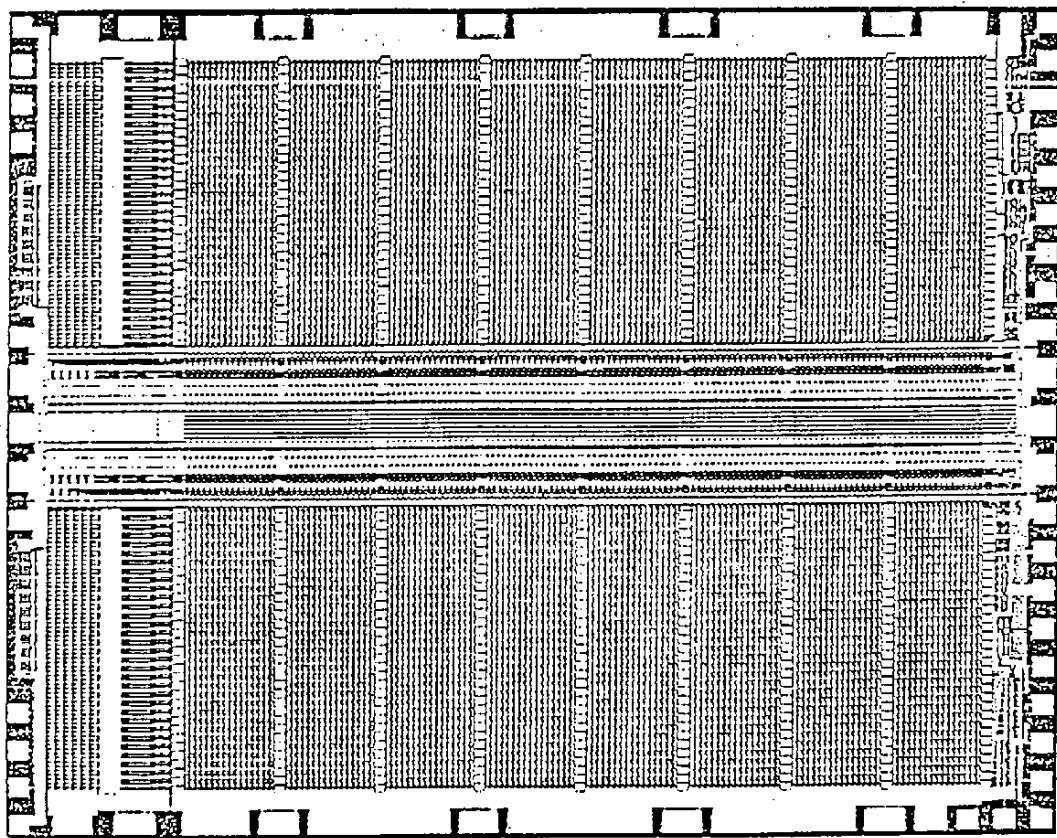
Microphotograph of 16 k SRAM

Microphotograph of 4.1 k gate array

Γ L

B C

E

| N | P$^+$ | i | P$^+$ | n$^+$ |
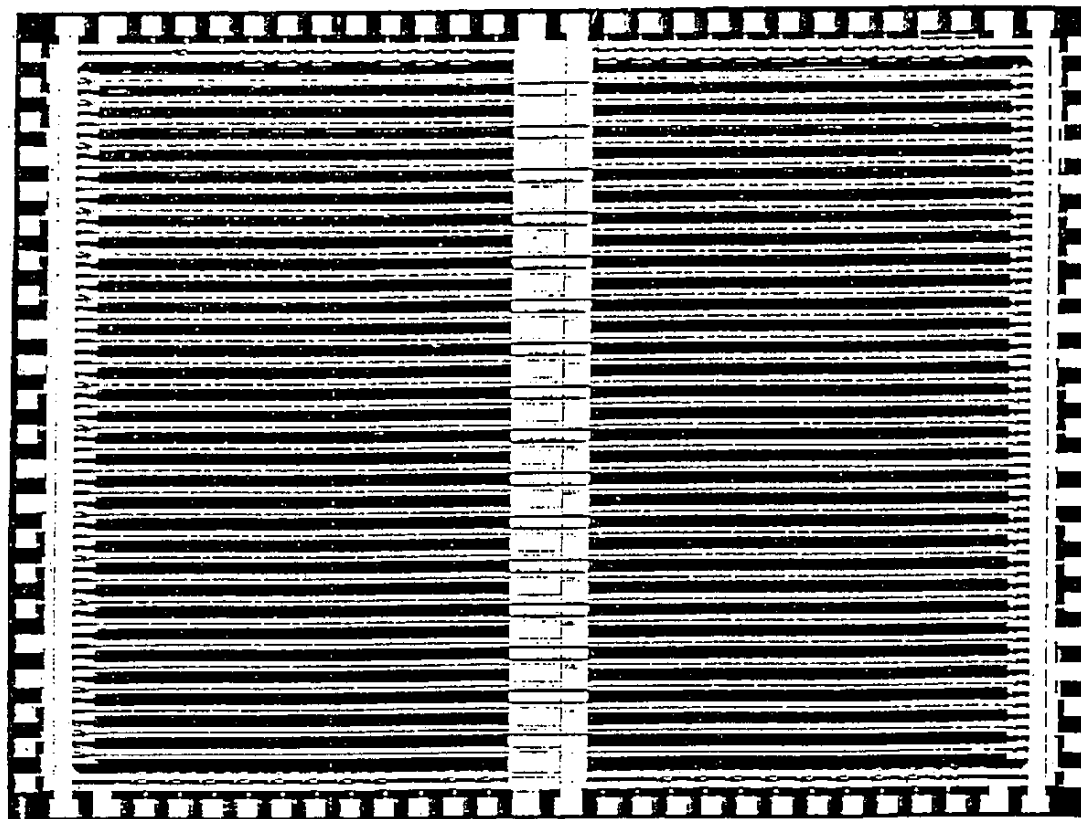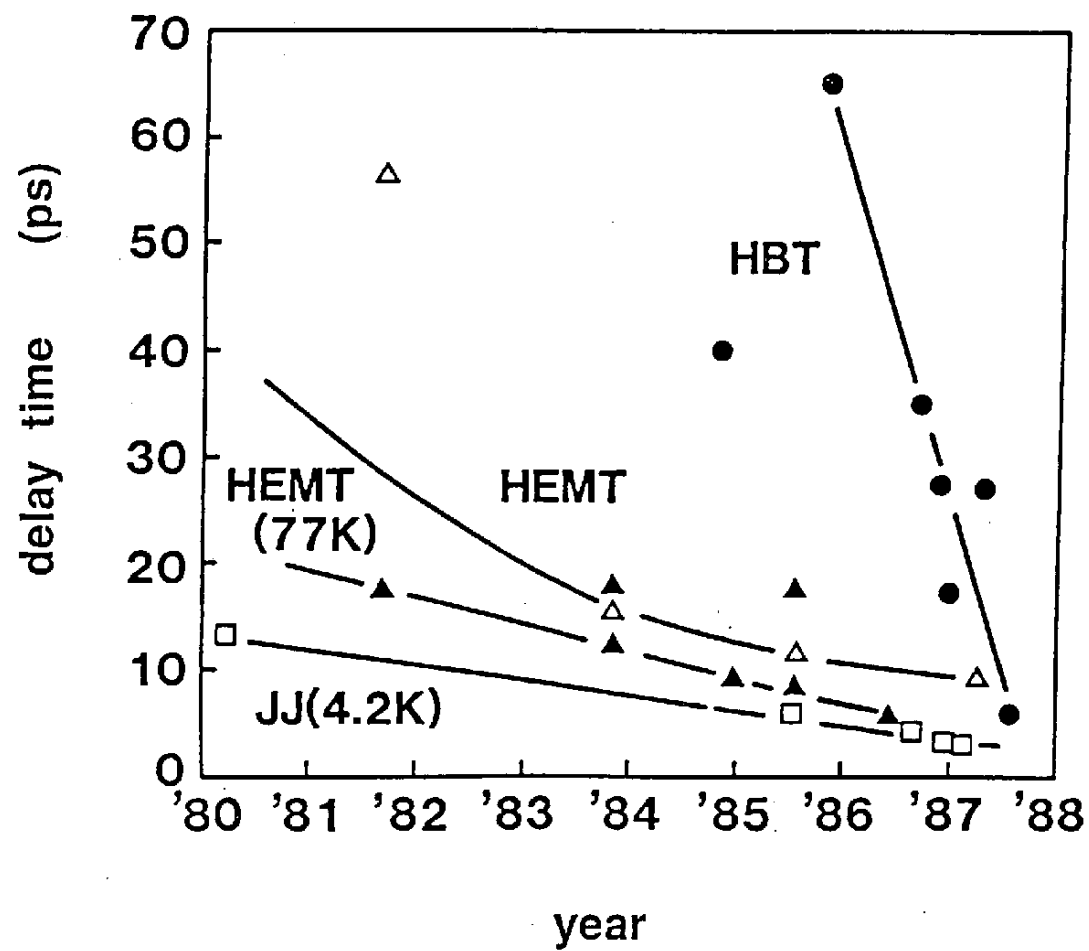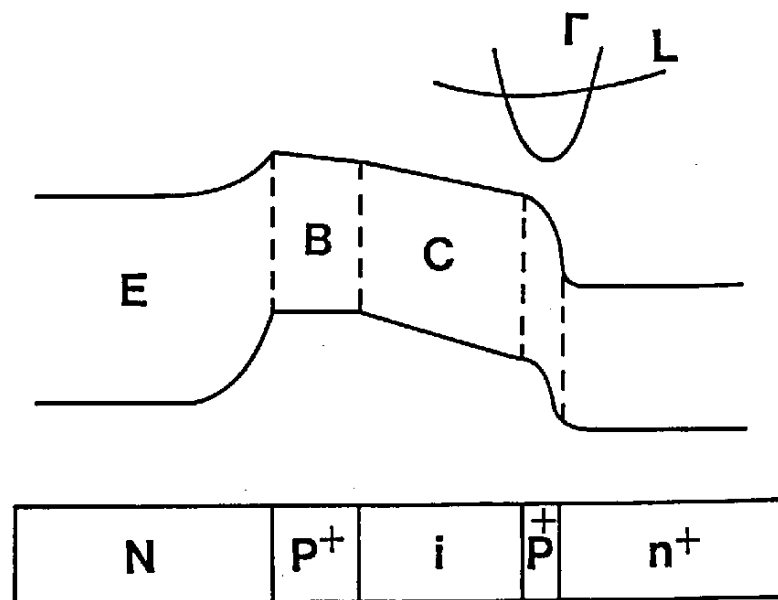
Device strucure and correspondencing
enegy band-diagram
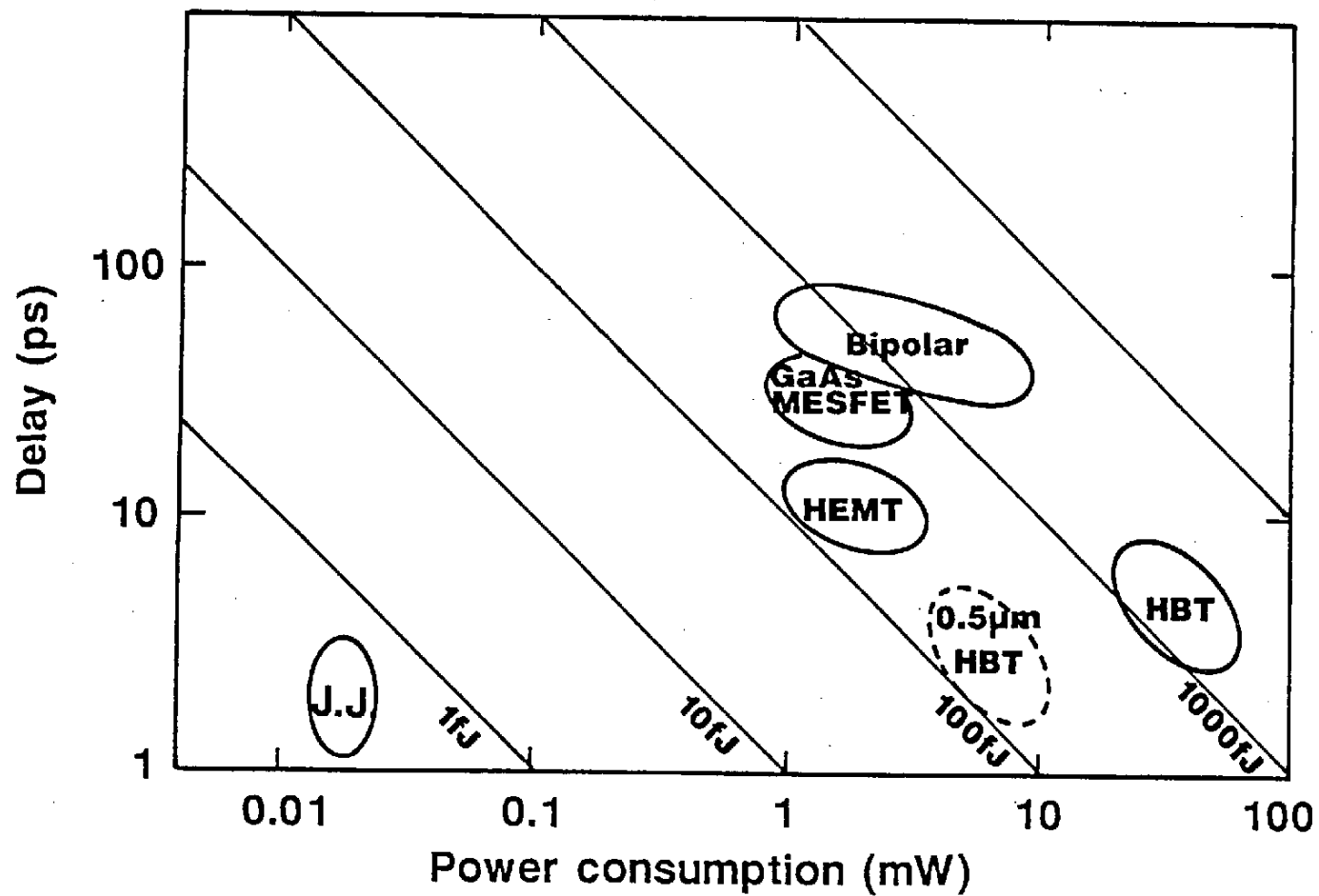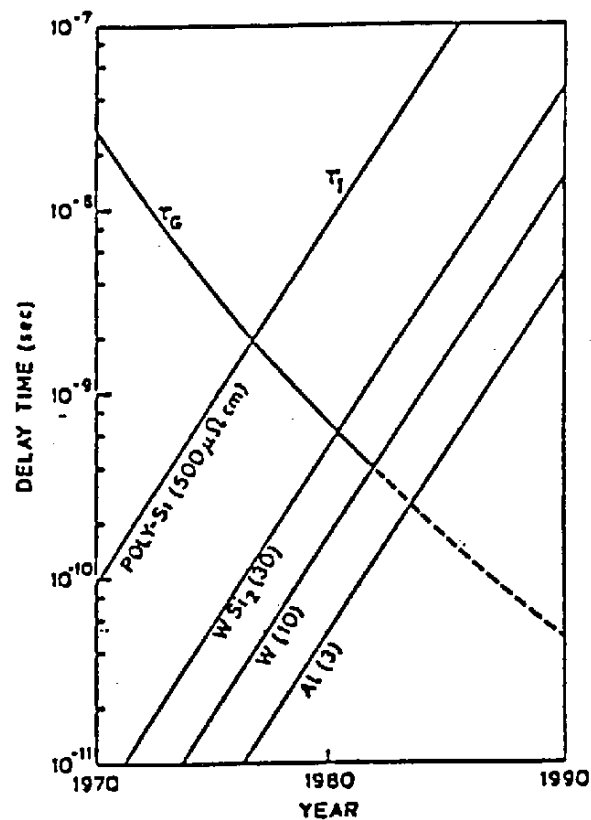
Interconnection time delay and average gate delay versus year of fabrication for the state-of-the-art chip fabricated that year.
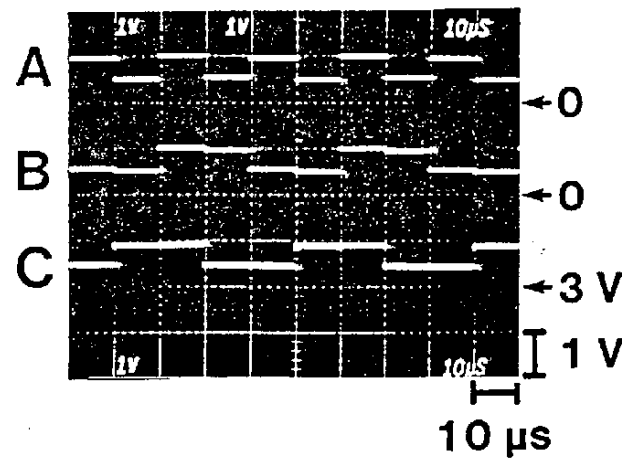
$\tau_{e-c} < 1\,p\,s,\quad J_{peak} = 1 \times 10^{5}\ A/cm^{2}$

HOT ELECTRON

E

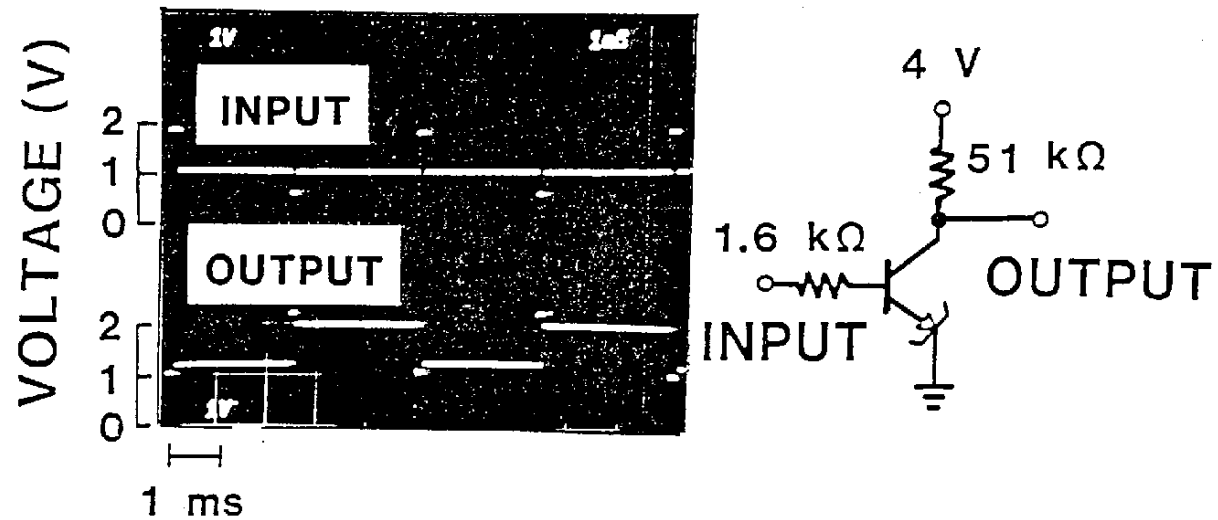n-GaAs

B

n-GaAs

AIGaAs

C

n-GaAs

$I_C - V_{BE}$

$I_C - V_{BE}$
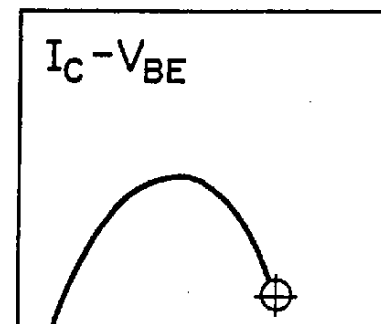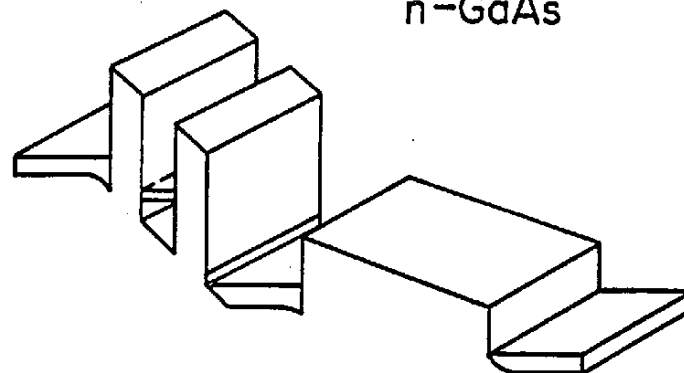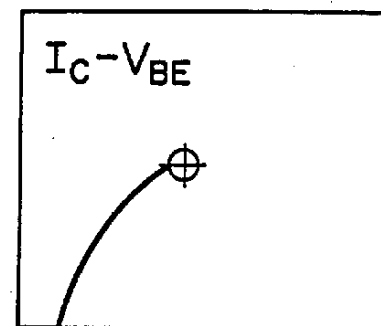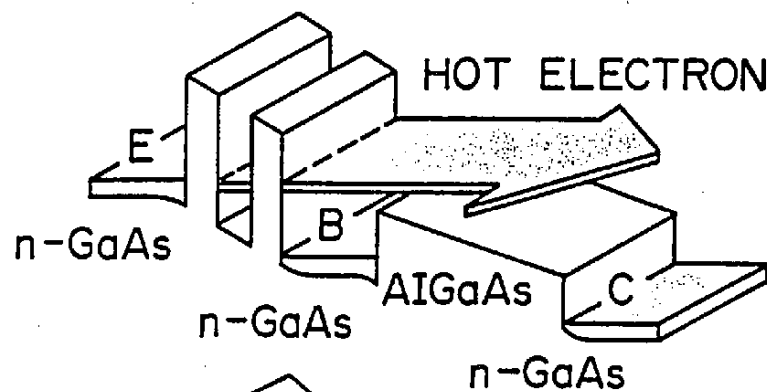
Operating principle of the RHET

EXCLUSIVE-NOR LOGIC FUNCTION

10 µs
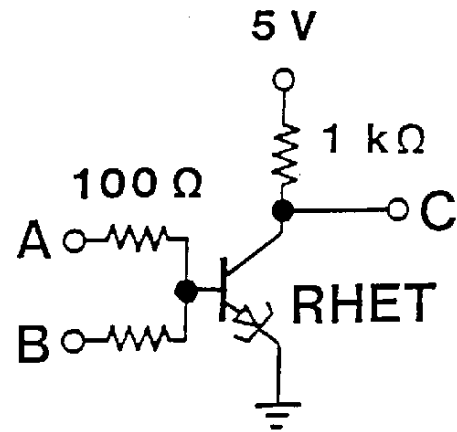
FLIP-FLOP FUNCTION

Summary

1. Low noise HEMT
   - Satellite communications
   - Radio astronomy

2. HEMT LSI's
   - A 16 k bit static RAM
   - A 4.1 k gate array
   - The project on Super Computer

3. HBT's
   - Delay time : 2.6 ps.
   - Power consumption : 60 mW/gate

4. RHET's
   - New functions
   - Large-scale and high density circuits

Subpicosecond Silicon Opto-Electronic Switches

M.Lambsdorff and J.Kuhl

Max-Planck-Institut für Festkörperforschung, Heisenbergstr.1
D-7000 Stuttgart 80, Federal Republic of Germany

E.Lopez, H.Leier,A.Forchel

IV.Physikalisches Institut,Universität Stuttgart, Pfaffenwaldring 57
D-7000 Stuttgart 80, Federal Republic of Germany

The topic of our research is the conversion of ultrashort optical pulses into ultrashort electrical pulses. This task is accomplished by the illumination of photoconductive silicon on sapphire (SOS) with femtosecond laser pulses. The SOS must, however, possess ultrashort free carrier lifetimes which we ensured by ion implantation with variable dose ranging between 3×10^{12} and 3×10^{15} Si^+ cm^{-2}. The deep level defects generated by the bombardment are known to act as highly efficient trap and recombination centers for optically generated carriers. We produced the electrical pulses by momentarily short-circuiting a charged coplanar transmission line /1/ (Fig.1) by illumination with 80 fs laser pulses derived from a hybridly mode-locked synchronously pumped dye laser (photon energy 2 eV).
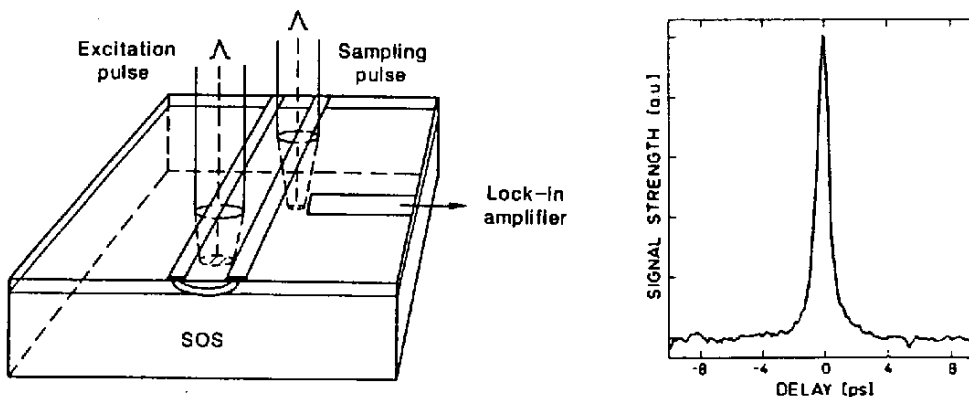

Fig.1: *Experimental configuration.*
Fig.2: *Optically sampled electrical cross-correlation obtained for an irradiation dose of $10^{15} Si^+ cm^{-2}$.*

The transmission line structure consists of two parallel 5μm wide and 0.5μm thick Al lines separated by 10μm (design impedance 100Ω) and fabricated by electron beam lithography. The beam of optical pulses is split into two. The shape of the electrical signal is measured by a photoconductive gap driven by a time-delayed sampling pulse (electrical cross-correlation). In Fig.2 we present the shortest electrical pulse, which we obtained from a switch with a Si^+ irradiation dose of 10^{15} cm^{-2}. From the full width at half maximum we determine a free carrier trapping time of 0.5 ps by deconvolution taking into account the finite response time of the electrical circuit, which is limited by the product of the gap capacitance (1 fF) and the line impedance. Figure 3a shows the dependence of free carrier lifetimes on implantation dose. For low implant levels, the carrier lifetimes decrease almost linearly with increasing implantation dose, whereas a saturation to 0.5 ps is observed at high implant levels. This result is consistent to former time-resolved reflectivity measurements /2/. We attribute the 500 fs-limit to the thermalization time of the photoexcited carriers (initial excess enery 0.5 eV) when they relax toward the mobility edge. The dependence of the extended-state mobility calculated from the signal intensity at delay zero on implantation dose is depicted in Fig.3b. The decrease with increasing implant levels indicates the increased elastic scattering from the neutral defects. The absolute values are significantly higher than those formerly obtained in completely amorphous silicon /3/. Even the highest implantation levels thus do not completely amorphize the silicon.
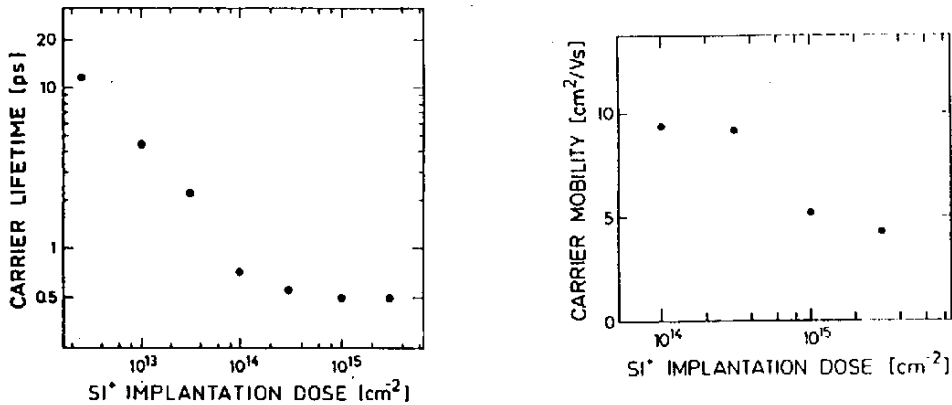

Fig.3: *Carrier lifetime (a) and extended-state mobility (b) in dependence on ion implantation dose. Lifetimes are derived from electrical cross-correlation data at each dose whereas mobilities are calculated from the measured signal intensity at zero delay.*

In the second part of this contribution, we want to discuss the propagation characteristics of ultrashort electrical pulses on coplanar transmission lines. Subpicosecond electrical pulses have more than 1 THz spectral bandwidth. Thus propagation leads to distortion

arising from dispersion and frequency-dependent losses. The so-called sliding-contact excitation /1/ allows us to analyze the propagation characteristics by continuously varying the distance between excitation and sampling spot (see Fig.1). The voltage pulse of Fig.2 is obtained for 100μm separation between exciting and sampling beams. As the distance is increased to 4 mm (Fig.4) propagation effects can be observed in a broadening of the correlation function to 2 ps. The dispersion of the
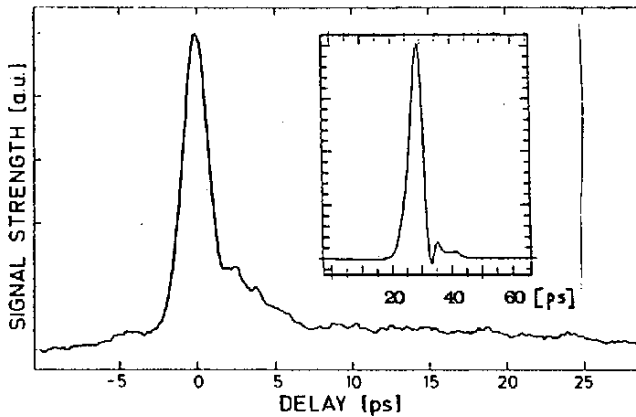

Fig.4: *Optically sampled cross-correlation for 4 mm separation between excitation and sampling spot. The inset shows the result of a model calculation described in the text.*

coplanar stripline can be expressed as the variation of the effective dielectric constant with frequency. When the pulse travels down the transmission line, the high frequency components are delayed because they encounter a higher effective dielectric constant. Frequency-dependent attenuation arises first from the increase of the line resistance with frequency due to the skin effect ($\sim\omega^{0.5}$) and second from radiation damping ($\sim\omega^3$). As the velocity of the subpicosecond pulse on the coplanar line exceeds the phase velocity of terahertz radiation in sapphire, the moving pulse emits an electromagnetic shock wave /3/ analogous to Cerenkov-radiation in electrooptic materials /4/. We developed a propagation model that takes dispersion and attenuation phenomena into account. The agreement between the model calculation, shown in the inset of Fig.4, and the experimental results is seen to be only qualitative. Quantitatively, the observed pulse dispersion is much weaker than expected theoretically. The reason for this discrepancy is not yet clear. We suppose that the applied theory of modal dispersion on coplanar transmission lines /6/ is only valid for frequencies$\langle$1 THz.

References

/1/ M.B.Ketchen, D.Grischkowski, T.C.Chen, C-C.Chi, I.N.Duling, III, N.J.Halas, J-M.Halbout, J.A.Kash, and G.P.Li, Appl.Phys.Lett. **48**, 751(1986).

/2/ F.E.Doany, D.Grischkowsky, and C.-C.Chi, Appl.Phys.Lett. **50**, 460(1987)

/3/ A.M.Johnson, D.H.Auston, P.R.Smith, J.C.Bean, J.P.Harbison, and A.C.Adams, Phys.Rev.B **23**, 6816(1981)

/4/ D.Grischkowski, I.N.Duling III, T.C.Chen, and C.-C.Chi, Phys.Rev.Lett. **59**, 1663(1987)

/5/ D.H.Auston, Appl.Phys.Lett. **43**, 713(1983)

/6/ G.Hasnain, A.Dienes, and J.R.Whinnery, IEEE Transactions on Microwave Theory and Techniques, MTT-**34**, 738(1986)

Silicon Bipolar Process and Device Technology for Very High Speed LSIs

Tetsushi Sakai

NTT LSI Laboratories

Nippon Telegraph and Telephone Corporation

3-1, Morinosato Wakamiya, Atsugi-shi, Kanagawa, 243-01 Japan

I. Introduction

Very high-speed LSIs are key components in information processing systems, such as main frame computers, optical transmission systems, and so on. From a practical standpoint, a silicon bipolar LSI is a very promising device because of its fast switching, high driving capability, high yield, and high reliability.
To achieve very high speed operation, several double-polysilicon self-aligned bipolar technologies have been developed to scale down lateral feature size and reduce parasitic capacitances and resistances. Using about 1μm lithography, 2kG masterslices with a basic gate delay time of 43~54ps/gate and a 64kb ECL RAM[6] with an access time of 2.3ns have been already been developed.
In this presentation, the structure, process and fundamental performance of the SST-1B integrated transistor and the application results for very high speed LSIs are described as one of several double-polysilicon self-aligned bipolar technologies. Moreover, future performance of bipolar LSI is examined by device simulation.

II. Device Structure and Process

A cross-sectional view of the SST-1B integrated transistor, which is almost the same as SST-1A, is shown in Fig.1. The main distinguishing feature of the SST-1B is the addition of a Selectivery Ion-Implanted Collector, or SIC. The N region is selectively located just under the intrinsic base region. The structure can be easily achieved by adoption of ion-implantation using the base polysilicon electrode as a mask in the conventional process flow of SST-1A. The SIC base width can be made 1.5 to 2 times smaller than the width of SST-1A due to carrier compensation for the base channeling tail. Furthermore, the SIC can suppress base pushout effect during high current density, as shown Fig.2.

Consequently, an improved cut-off frequency with higher current density can be expected without increasing base resistance and external base-collector capacitance.

III. Fundamental Performance

The measured cut-off frequency, f_T, versus collector current, Ic, are shown in Fig.3. Maximum f_{TS} of 21.1 GHz(V_{CE}=1V) and 25.7 GHz(V_{CE}=3V) have been achieved in comparison with 16.8 GHz and 20.2 GHz for SST-1A. In addition, the current density required to obtain maximum f_T increases by a factor of 2. Thus, the SST-1B transistor has large driving capability. Measured basic propagation delays, tpd, of NTL and ECL ring oscillators are shown in Fig.4. Minimum delayes of 20.5ps/gate for the NTL and 34.1 ps/gate for the ECL have been achieved.

IV. Application

Using SST-1B, we have developed various ICs for microwave application, high-speed analog application, and high-speed digital application. Characteristics of these ICs are shown in table 1. The performance of a 18 GHz 1/8 divider, a 2-Gbsps 6-bit flash AD converter, and a 43ps/5.2GHz macrocell array LSI are described in this section.

A. 18 GHz 1/8 divider

Since a Regenerative Frequency Divider, RFD, has a higher operating frequency than that of an ECL master-slave D-flip-flop with the output fed back to the data input, T-F/F has been used in a monolithic integrated circuit. The 1/8 dividers consists of the RFD as the first stage, two T-F/F's, two internal buffers, and an output buffer. The divider can operate smoothly for input frequencies from 4.6 GHz to 17.5 GHz under the designed bias condition with a power dissipation of 690mW. A maximum operating frequency of 18.0 GHz has been obtained by adjusting bias conditions as shown in Fig.5.

B. 2 Gbsps 6-Bit Flash AD conversion LSI

The dynamic performance was measured using GHz-operation data acquisition system developed with SST MSI family. The maximum sampling rate was more than 2 Gsps. Recent progress of the 6-bit AD converter development is shown Fig.6. A 1-GHz sampling rate has already been achieved with a hybrid IC using GaAs and Si bipolar LSIs, but it has a large power dissipation of more than 10W. In the LSI

which we developed, a sampling rate was twice that of the hybrid IC with a low power dissipation of 2W.

C. 43ps/5.2GHz 2.1kG macrocell array LSI

The 2.1kG macrocell array has 324 internal cells, 136 I/O cells, and 1062 wiring channels, and uses one supply voltage: -3V for V_{EE}. A basic cell consists of 16 transistors, and 28 resistors. The performance of this macrocell array LSI is summarized in Table II. To evaluate the macrocell array LSIs, a 16 bit multiplier was fabricated. Multiplication time of 4.3 ns was obtained. The power consumption was 3W. The speed of the 16-bit multiplier is almost the same as that of the HEMT device, which was reported at the 1987 CICC, and the power dissipation of the multiplier is 1/2 times smaller than that of the HEMT device.

V. Future Performance of Silicon Bipolar LSI

Sensitivities of the SST-1B device parameters were caluculated using SPICE-II to examine how to further reduced propagation delay. Transit time, collector-base capacitance and base resistance have high sensitivities of 56%, 35% and 30 %, respectively. For high speed switching, and especially transit time or cut-off frequency the SST-1B is most effective. A 40-50 GHz silicon bipolar transistor with 40nm base width is expected as a result of two dimentional device simulation. Utilization of a Si hetero-emitter junction makes it possible to achieve a f_T of more than 100 GHz by reducing the base width to about 10nm. Using double-polysilicon self-aligned bipolar technology with lithography of less than a halfmicron, half-50ps/gate 2~3kG silicon bipolar masterslice LSI will be realized in the future. Very high performance VLSI with bipolar and CMOS of less than a halfmocron rule will be also realized. One of the most important problems in process and device design is the reduction of ohmic contact resistance. An advance in LSI design is the development of CAD with design of crosstalk, timing and so on.

Table I. Characteristics of various LSIs by using SST

Variety	Charateristics	Variety	Charateristics
Macrocell array LSIs (1KG, 2.1KG)	Propagation delay time D-ECL 43ps/G, ECL 54ps/G F/F toggle frequency 5.2GHz	6b A/D converter	Operation speed 2Gs/s Power dissipation 2W
16b multiplier	Multiplication time 4.3ns Power dissipation 3W	1/8 divider (dynamic)	Max. operation freq. 18GHz Power dissipation 644mW
6b multiplier	Multiplication time 1.2ns Power dissipation 1.2W	Prescaler	Max. operation freq. 2.2GHz Power dissipation 22mW
Exchange time switch 4-multiple 2-highway	Max. operation freq. 3.3GHz Power dissipation 1.3W	Amplifier Pre.+buffer Pre. Pre.	DC-3.5GHz 30dB DC-3.2GHz 20dB DC~5.5GHz 16.4dB
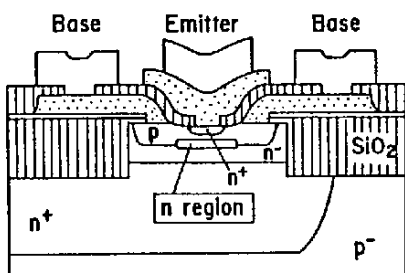
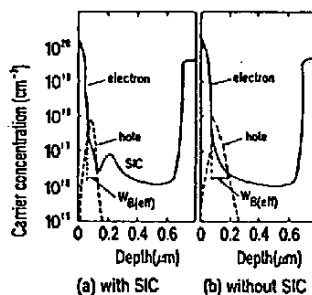Fig.1. Cross-sectional view of the SST-1B.

(a) with SIC   (b) without SIC

Fig.2. Calculated carrier profiles (a)with SIC, and (b) without SIC at 40KA/cm^2.
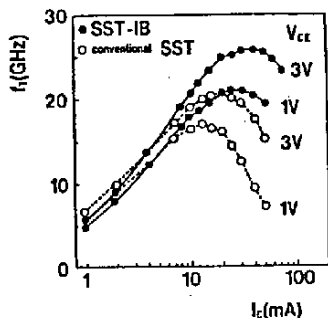
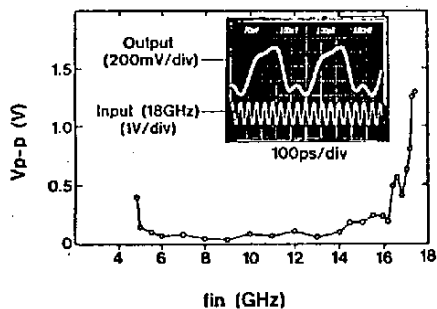Fig.3. Measured f_T-I_C curves at V_{CE}=1V and 3V for SST-1B(Solid) and SST-1A(Dashed).

Fig.4. Basic gate delays of NTL and ECL using SST-1B(Solid) and SST-1A(Dashed).

Fig.5. Input sensitivity vs. input frequency, and waveforms at 18.0 GHz.

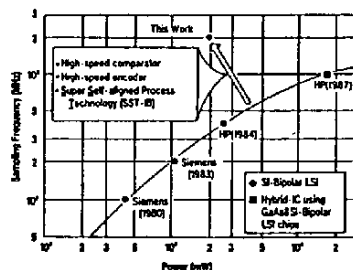Fig.6. Recent progress of the 6-bit AD coverter.

Table II. Summary of the measured results of the cell performance.

Basic Delay (Single–Ended)	54 ps
(Differential)	43 ps
Fan–Out Delay	6 ps/FO
Fan–In Delay	20 ps/FI
Series–Gate Delay	20 ps/SG
Metal Delay	13 ps/mm
F/F Toggle Frequency	5.2GHz

PRESENT STATUS AND FUTURE PERSPECTIVE
OF ULSI MOS DEVICES

Eiji Takeda

Central Research Laboratory, Hitachi Ltd.
Kokubunji, Tokyo 185, JAPAN

"ULSI revolution" marking a new epoch in the electronic industry has made remarkable progress to such an extent that 10^7-10^8 transistors are fabricated on a single chip. For instance, current ULSI microfabrication technologies are being pushed to the extremes by the DRAM community, hereby expediting research on 64 Mbit DRAMs using a 0.3 μm design rule. Since process and device technologies in such a deep submicron region are, however, approaching practical limits, reliability problems as well as improvement of performance are becoming increasingly significant. In particular, the scaled MOSFET (ULSI building element) is suffering from such high field effects as hot-carrier effects and the down-sliding of scaling merit. This trend requires a deeper physical insight into new reliability problems in the deep submicron region(0.5 - 0.1 μm) and feedback of this knowledge to device structures and circuit design.

In this paper, the state-of-the-art and future perspective of MOS devices are reviewed and discussed from the viewpoint of: 1) hot-carrier and short-channel effects, 2) device structures with high reliability and improved performance, 3) future power supply voltage, 4) new reliability problems in ~ 0.3 μm region, and 5) Si quantum effects in the region less than 0.1 μm.

Firstly, device structures and hot-carrier breakdown voltage for each DRAM generation are shown in Fig. 1. Several kinds of hot-carrier resistant device structures such as DDD[1] and LDD[2], have been proposed so far, but a 5 V supply voltage can not be used even in LDD with L_{EFF} less than 0.8 μm. Therefore, in the era of 0.5 - 0.3 μm, two approaches will be taken according to the type and purpose of ULSIs. These are: ① new hot-carrier resistant devices[3-4] usable with a 5 V supply, and ② reduction of power supply voltage (3-1.5 V). In the former approach, a deeper physical understanding of high field effects such as hot-carrier and short channel-effects is needed and the power consumption problem[5] becomes significant. The latter must also overcome a low speed problem because subthreshold voltage can not be scaled, resulting in the low channel current. Optimal device operation for any ULSI device can be achieved by choosing the best hot-carrier-resistant device structure so subsequent discussions will emphasize

on the relevant characteristics of these structures. At any rate, it will be important to secure maximum total performance by putting suitable devices in the right places of ULSIs.

With regards to hot-carrier(HC) effects, primary attention is now paid to device degradation under the pulse(AC) stress corresponding to actual circuit operation. Device life-time(τ_{AC}) under AC stress has been shown to be related to effective DC stress time by $\tau_{AC} = \tau_{DC} \cdot R[6]$, where R is a circuit duty ratio, but recently discovered device degradations specific to AC stress requires a re-examination of this equation. Main experimental results[7-9] are summarized in Table 1. Carrier trap-detrapping effects and/or excess carrier generation at pulse fall/rise periods cause degradation enhancement and device structure dependent phenomena to occur. The device life-times in both single drain(SD) and LDD are shown as a function of substrate current(I_{SUB}) in Fig. 2, comparing AC with DC stress. It can be seen that τ_{AC} strongly depends on the device structure, leading to the equation: $\tau_{AC} = \alpha \cdot \tau_{DC} \cdot R$, where α is a function of device structure. These experimental results seem to be due to electric field modulation by carrier trap-detrapping effect under AC stress condition. From now on, hot-carrier effects will reveal new facets in ULSI reliability; HC effects under low voltage[10], HC effects vs. elecro-static discharge(ESD)[11], HC effects vs. TDDB[12], to name a few.

With a low power supply voltage(1.5-3 V), short-channel effects such as punch-through(V_{TH}-lowering), rather than HC effects, are more important in the deep submicron device design. This is because source-drain depletion width is comparable to channel length, resulting in gate-uncontrollabilty to channel region. The allowable effective channel length(L_{EFF}) is shown in Fig. 3 as a function of gate oxide thickness(T_{OX}) with V_{TH} as a parameter. A decrease of T_{OX} and increase of channel dose is ineffective against punchthrough in the deep submicron region. Rather, down-scaling of source-drain junction depth ($< 0.1\ \mu$m) and channel stopper are more effective. Moreover, the thin film SOI structure[13] becomes important as a ULSI element because this device has good characteristics such as suppressed V_{TH}-lowering and non-floating effect of substrate.

Inversed-T[4] and GOLD[3], which make good use of gate-drain overlapped(GOLD) effect[14], have been reported as MOS device structures usable with a 5 V supply voltage. A typical GOLD structure is shown in Fig. 4. In such GOLD structures, not only high resistance against HC effects, but also high transconductance are realized in 0.3-0.5 μm regions as shown in Fig. 1. This high performance is essentially due to a decreased source resistance due to the GOLD effect. Thus, consistence of reliability and performance will make the GOLD structures more suitable for Bi-CMOS ULSIs and high-end computers aimed at high speed.

High power consumption problem in ULSIs requires the power supply reduction. Unfortunately this results in a degradation of ULSI speed since velocity saturation and decreased effective mobility due to vertical electric field, as well as low channel current caused by low gate voltage occurs. To overcome these problems, it is imperative to eliminate such parasitic elements as junction capacitance and contact resistance by using sophisticated self-align technologies [15] and SOI technology. In particular, the SOI structure with < 0.1 μm thin substrate will become more important as a ULSI building element because it can avoid a substrate-floating problem inherent to conventional SOIs. In addition, the low temperature operation[16] is attractive under low supply voltages because subthreshold characteristics are remarkably improved, which enables V_{TH} to be scaled down.

In the deep submicron era (~0.3 μm), new reliability problems emerge with the reduction of device dimensions as shown in Table 2. Among them, main problems are as follows: ① Alpha-particle induced source/drain penetration(ALPEN) effect[17], ② Band to band tunneling effect[18], and ③ n⁻ source/drain penetration effect[19].

ALPEN effect is a type of punchthrough caused when L_{EFF} becomes comparable to funneling length (electric field distortion due to α-particle injection). This effect causes various constraints such as new soft error in ULSI memories and latch-up.

The gate-induced band to band tunneling results in drain leakage current, which demands LDD structure, rather than SD even under a 3 V supply voltage. This phenomenon occurs when T_{ox} < 10 nm. Also, this is reported to cause a new hot-carrier effect[20] in which holes generated by band to band tunneling are accelerated and injected into the gate oxide, leading to V_{TH} decrease. A larger channel dose is needed to taylor V_{TH} with reduced L_{EFF}. This higher channel impurity concentration(~10^{18}cm⁻³) causes compensation of n⁻ region in LDD.

As device dimensions(< 0.1 μm) become comparable to electron wave length (the De Blois wave length), quantum phenomena emerge even in Si. Preliminary research on quantum effects in Si has begun for the purpose of discovering new phenomena related to ULSI reliability, rather than for proposing new quantum devices. These play a "warning" role for future ULSIs. The following phenomena have been reported as predominant quantum effects(size effects) in Si: ① impurity fluctuation[21] $\Rightarrow$ V_{TH} scattering, ② single electron trapping[22] $\Rightarrow$ channel current scattering, ③ velocity overshoot[23] $\Rightarrow$ channel current increase, and ④ abnormal conductance in one-dimensional electron system[24] $\Rightarrow$ G_m oscillation.

Although all phenomena except velocity overshoot are found to be related to

reliabilty, these effects may trigger new quantum devices. Already, the single electron transistor, which makes good use of single electron trapping into gate oxide, has been proposed.

Since the De Blois wave length in Si is smaller than that in GaAs, it seems to be more difficult to construct Si quantum devices. However, considering high quality Si crystal and advanced Si ULSI production technologies, Si quantum ULSIs could be realized. If so, the impact to electronic industry will be remarkable and a new GSI (Giga Scale Integration) revolution will come into existence. Therefore, to achieve such a marked progress, device innovation is strongly required.

Reference

[1] E. Takeda et al., IEEE Trans. Electron Devices, ED-30, p. 652, 1983.

[2] S. Ogura et al., IEEE Trans. Electron Devices, ED-27, p. 1359, 1980.

[3] R. Izawa et al., IEEE IEDM, pp. 38-41, 1987.

[4] T. Huang et al., IEEE IEDM, p. 742, 1986.

[5] K. Kimura et al., IEEE J. Solid-State Circuits, SC-21, p. 381, 1986.

[6] T. Sakurai et al., IEEE ISSCC, pp. 272-273, 1985.

[7] Y. Igura et al., 1987 Symp. on VLSI Technology, pp. 47-48.

[8] J.Y. Choi, et al., 1987 Symp. on VLSI Technology, pp. 45-46.

[9] W. Weber, IEEE TRans. Electron Devices, ED-35, pp. 1476-1486, 1988.

[10] E. Takeda et al., IEEE IEDM pp. 396-399, 1983.

[11] S. Aur et al., 1988 Intn. Reliability Phys. Symp., pp. 15-18.

[12] I.C. Chen et al., 1988 Intn. Reliability Phys. Symp. pp. 1-7.

[13] J.-P. Colinge, IEEE Electron Device Letters, EDL-6, pp. 573-575, 1985.

[14] R. Izawa et al., IEEE Electron Device Letters, EDL-8, pp. 480-482, 1987.

[15] W.T. Lynch, IEEE IEDM, pp. 354-357, 1987.

[16] F.H. Geaensslen et al., IEEE Trans. Electron Devices, ED-24, p. 218, 1977.

[17] E. Takeda et al., 1988 Intn. Reliability Phys. Symp., pp. 109-112.

[18] T.Y. Chan et al., IEEE IEDM, pp. 718-721, 1987.

[19] A. Hamada, IEEE Electron Device Letters, EDL-8, pp. 398-400, 1987.

[20] H. Matsuoka et al., Extended abstract of the 20th SSD&M, p. 589, 1988.

[21] R.W. Keyes, Proceeding of the IEEE, vol. 63, p. 740, 1975.

[22] W.J. Skocpol et al., Phys. Rev. Lett. p. 2865, 1986.

[23] S.Y. Chou et al., IEEE Electron Device Letters, EDL-6, p. 665, 1985.

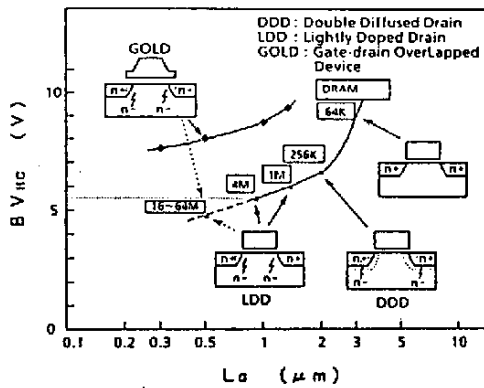[24] Y. Katayama et al., Surface Sci., vol. 170, p. 28, 1986.

Fig.1 Device structure and hot carrier
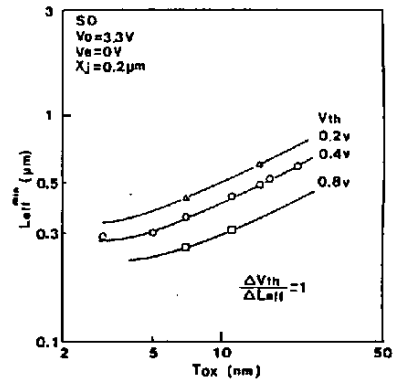breakdown voltage for each DRAM
generation

Fig.3 The allowable effective channel
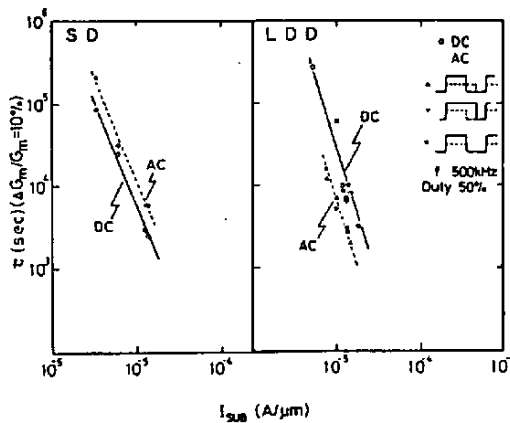length vs. gate oxide thickness
with Vth as a parameter

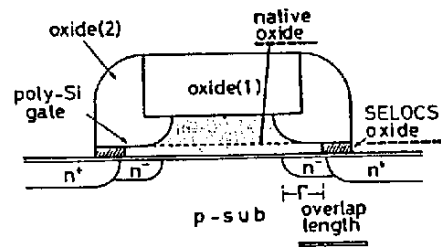Fig.2 Substrate current vs. hot carrier
lifetime both in SD and LDD

Fig.4 A typical GOLD structure

Table 1 AC stress experimental results

	HITACHI	UCB	Siemens
Experimental results under AC stress	·Device structure dependence ·Suppressed in As-D and enhanced in LDD	·Enhanced in the falling period of Vg (Vd:large) ·In other cases, no difference between AC and DC stress	·Enhanced when plasma nitride is used as a passivation layer ·Device structure dependence
AC stress degradation mechanism	·Electric field modulation due to electron detrapping	·Excess carriers (hole) in the channel region cause the degradation at large Vd	·Electric field modulation due to hole detrapping

Table 2 ULSI reliability problems and power supply voltage

Minimum length (μ m)			10	1	0.1
Supply Voltage			12 V	5 V	3 V 1.5 V
High electric field effect	Gate oxide	TDDB (FN tunnelig)		Thin oxide (~5 nm)	
	Device	Hot carrier effect		DDD → LDD → GOLD	
		α particle soft error		ALPEN effect	
		Short channel effect		Punch-through	
		Band to band tunneling			Band to band tunneling
Quantum effect	Random fluctuations of impurity numbers				Fluctuation of Vth
	Single electron trapping				1/f noise
	Velocity overshoot				High speed device
	Quasi one dimensional conductance oscillation				Oscillation of Gm

LOW TEMPERATURE MOLECULAR BEAM EPITAXY OF SILICON (Si-MBE)

E. Kasper

AEG Research Center Ulm, Sedanstr. 10, D-7900 Ulm, FRG

1. Introduction

The single crystal growth, by molecular beam epitaxy, of materials com-patible with silicon is described, and device applications are given. Process temperatures are decreased to 240 °C, heterojunction devices are fabricated, strained layer Si/Ge superlattices are investigated, and si-licon based monolithic integration of heterojunction devices and conven-tional devices is suggested.

2. Growth by Silicon Molecular Beam Epitaxy (Si-MBE)

By MBE the growth temperature of Si was already dramatically reduced compared to standard chemical vapour deposition (CVD) epitaxy. The MBE process sequence contains three main steps, namely (i) chemical pretreat-ment of the surface outside the growth apparatus, (ii) in situ cleaning of the substrate surface, and (iii) growth of the thin single crystal-line layer by condensation from impinging molecular beams of the matrix and dopant elements. In standard Si-MBE growth occurs usually between 550 °C and 800 °C. For this investigation we employed also very low growth temperatures below 550 °C.

To understand one has to consider the adsorption of the molecular beams on the growing surface. The surface consists (Fig. 1) of flat terraces bordered by atomic steps. The binding energy W (4.55 eV/Si atom) will be gained by sticking an atom on a kink of the step. But more frequently the impinging atom is adsorbed on the terrace. The adsorbed atoms move

rather easily on the surface like a twodimensional adatom gas. A diffu-
sing net flux of adatoms is directed toward the steps because these act
as sinks for adatoms. The steps move forward by catching the adatoms.
Macroscopic vertical growth is driven by the microscopic lateral motion
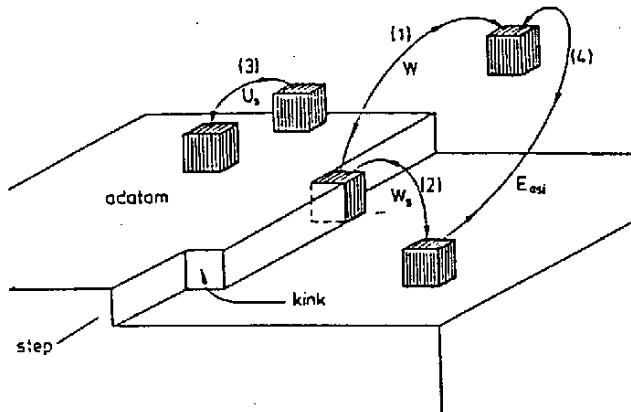of atomic steps.

Fig. 1: Condensation of molecular beams on a growing surface with
atomically flat terraces between atomic steps

Single crystalline growth of the silicon matrix is selforganized if not
the experimentalist disturbs the growth by freeze out of the surface mo-
bility (growth temperature below T_{em}) or by contaminating the surface
(inproper vacuum conditions).

3. Device Examples
Worldwide realized device types include bipolar IC s, discrete high fre-
quency diodes, waveguide optoreceivers, heterojunction transisitors and
resonant tunnelling elements. We discuss in more detail silicon mm-wave
(100 GHz) integrated circuits (SIMMWIC) and n-channel SiGe/Si MODFET's.

4. Strained layer SiGe/Si superlattices

Periodic stackings of heterostructures (superlattices) open the possibility to tailor material properties of semiconductors (artificial semiconductor). Material partners with lattice mismatch can be combined without crystal perfection degradation, if the superlattice period is thin (strained layer superlattices - SLS). The most prominent Si-based SLS system is the SiGe alloy with up to 4 % lattice mismatch. Adjustment of strain, mobility enhancement of holes and electrons, strain induced band ordering and phonon zone folding effects were already demonstrated in this system.

Most spectacular predictions promise for ultrathin Si/Ge superlattices a strong enhancement of direct band gap transitions. This would allow novel optoelectronic functions in a silicon based material system.

In strain symmetrized ultrathin Si/Ge superlattices on Si substrates superlattice related photoluminescence (PL) (Fig. 2) appears not found in alloy reference samples.
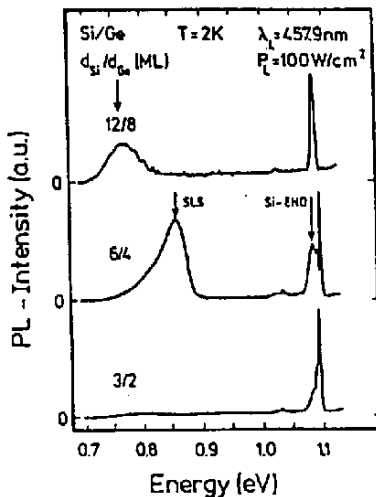

Fig. 2a: PL-spectra of the 3/2 ML,
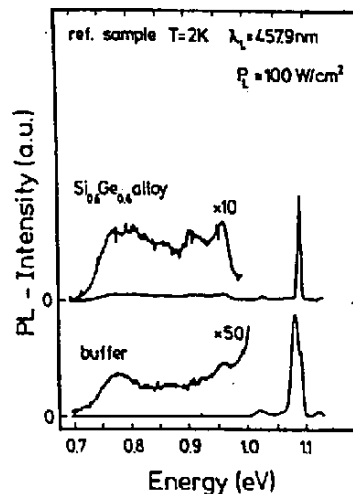6/4 ML and 12/8 ML Si/Ge-SLS
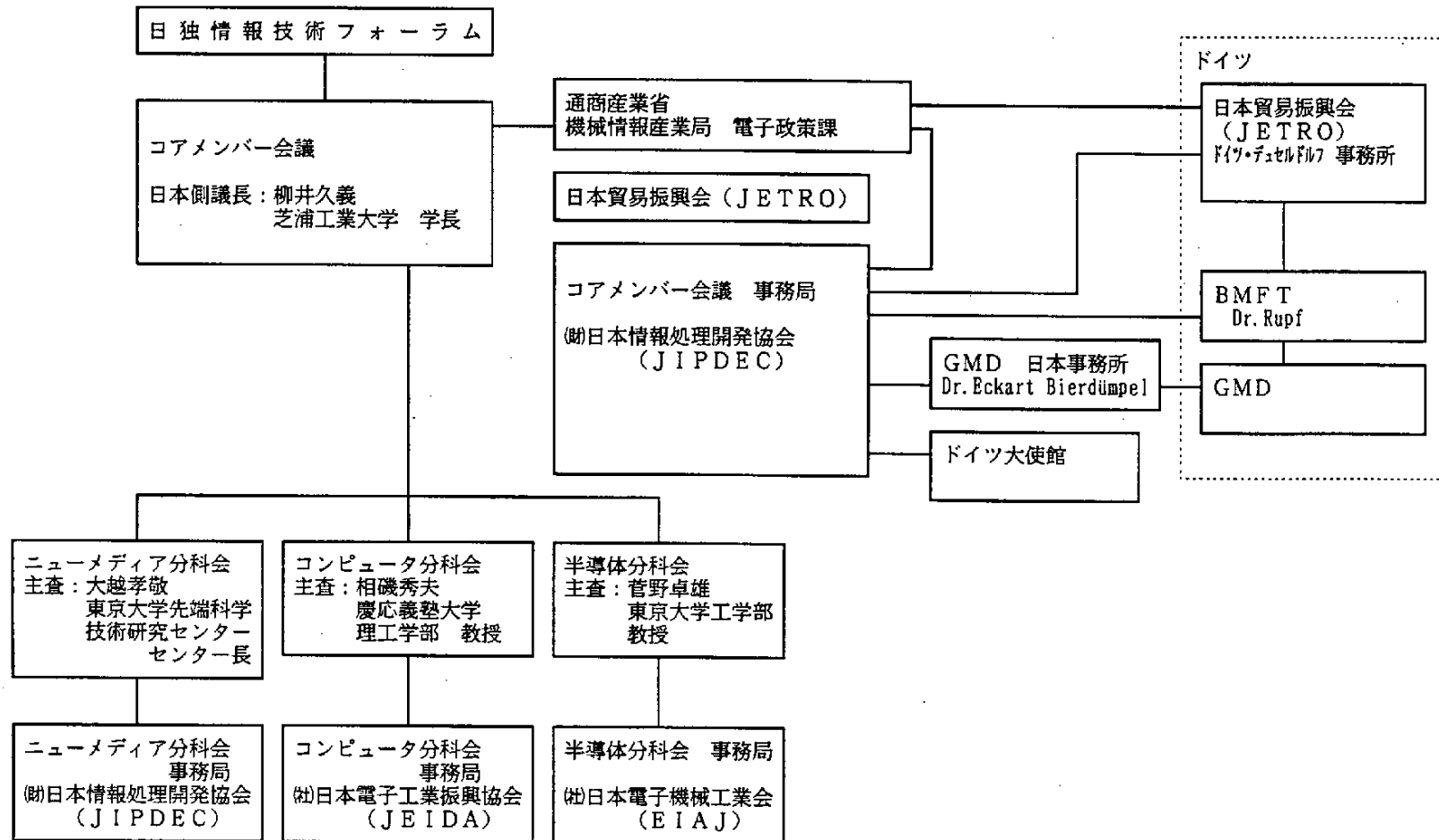
Fig. 2b: PL-spectra of the
reference samples

付録 5　日独情報技術フォーラム体制

付録 5 日独情報技術フォーラム体制

```
┌─────────────────────────────┐                                                    ┌ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┐
│ 日 独 情 報 技 術 フ ォ ー ラ ム │                                                     ドイツ
└──────────────┬──────────────┘                                                   │                           │
               │              ┌──────────────────────────┐         ┌──────────────────────┐
┌──────────────┴──────────────┐ │ 通商産業省                │         │ 日本貿易振興会          │ │
│ コアメンバー会議                │ │ 機械情報産業局  電子政策課    │         │ （ＪＥＴＲＯ）          │
│                             │─┤                          │         │ ﾄﾞｲﾂ・ﾃﾞｭｾﾙﾄﾞﾙﾌ 事務所    │ │
│ 日本側議長：柳井久義            │ └──────────────────────────┘         └──────────────────────┘
│        芝浦工業大学  学長      │ ┌──────────────────────────┐                               │
└──────────────┬──────────────┘ │ 日本貿易振興会（ＪＥＴＲＯ）  │                               │
               │                └──────────────────────────┘         ┌──────────────────────┐ │
               │                ┌──────────────────────────┐         │ ＢＭＦＴ                │
               │                │ コアメンバー会議  事務局      │         │ Dr.Rupf                │ │
               │                │                          │─────────└──────────────────────┘
               │                │ ㈶日本情報処理開発協会        │  ┌────────────────────────┐    │
               │                │ （ＪＩＰＤＥＣ）            │  │ GMD  日本事務所          │ ┌────────┐
               │                │                          │──│ Dr.Eckart Bierdümpel    │─│ GMD    │ │
               │                └──────────────────────────┘  └────────────────────────┘ └────────┘
               │                                              ┌────────────┐                │
               │                                              │ ドイツ大使館  │
               │                                              └────────────┘               └ ─ ─ ─ ─ ─ ─ ┘
```

ニューメディア分科会	コンピュータ分科会	半導体分科会
主査：大越孝敬 東京大学先端科学 技術研究センター センター長	主査：相磯秀夫 慶応義塾大学 理工学部 教授	主査：菅野卓雄 東京大学工学部 教授
ニューメディア分科会 事務局 ㈶日本情報処理開発協会 （ＪＩＰＤＥＣ）	コンピュータ分科会 事務局 ㈳日本電子工業振興協会 （ＪＥＩＤＡ）	半導体分科会 事務局 ㈳日本電子機械工業会 （ＥＩＡＪ）

1988年度「日独情報技術フォーラム，コアメンバー」（日本側）

議 長　柳 井 久 義　芝浦工業大学　学長

ニューメディア
　主査　大 越 孝 敬　東京大学　教授
　　　　　　　　　　　先端科学技術研究センター　センター長
　　　　戸 田　　巌　日本電信電話株式会社　研究開発技術本部
　　　　　　　　　　　常務取締役　本部長
　　　　辻 井 重 男　東京工業大学　工学部電気電子工学科　教授
　　　　沢 辺 栄 一　日本放送協会　放送技術研究所　研究主幹

コンピュータ
　主査　相 磯 秀 夫　慶応義塾大学　理工学部　教授
　　　　　　　　　　　情報科学研究所　所長
　　　　大 野　　豊　京都大学工学部　名誉教授
　　　　　　　　　　　甲子園大学　教授
　　　　　　　　　　　京都高度技術研究所　所長
　　　　柏 木　　寛　電子技術総合研究所　次長
　　　　田 中 英 彦　東京大学　工学部電気工学科　教授

半 導 体
　主査　菅 野 卓 雄　東京大学　工学部電子工学科　教授
　　　　田 中 昭 二　東京大学　工学部物理工学科　名誉教授
　　　　　　　　　　　東海大学　理学部物理学科　教授
　　　　　　　　　　　㈶国際超電導産業技術研究センター　副理事長
　　　　末 松 安 晴　東京工業大学　工学部　電子物理工学科　教授
　　　　佐々木 昭 夫　京都大学　工学部電気工学科　教授
　　　　徳 山　　巍　筑波大学　物理工学系　教授

1988年度「日独情報技術フォーラム・コアメンバー」（ドイツ側）

議　長　　Prof. Dr. Engl, Technology Univ. of Aachen

ニューメディア分科会

主査　　Prof. Baack, HHI

Prof. Kaiser, Univ. of Stuttgart

Dr. Raubold, GMD

Mr. Steiner, BMP

コンピュータ分科会

主査　　Prof. Goos, GMD

Prof. Steusloff, Fhg

Prof. Szyperski, Mannesmann

Prof. Giloi, GMD

半導体分科会

主査　　Prof. Queisser, MPI

Prof. Rupprecht, Fhg Freiburg

Prof. Heuberger, Fhg Berlin

Dr. Weyrich, Siemens

付録 6　第 5 回日独情報技術フォーラム・プログラム

付録 6. 第 5 回 日独情報技術フォーラム・プログラム

Schedule of the 5th Japan-Germany Forum
on Information Technology

I. Plenary Session

TUESDAY, NOVEMBER 22ND

Technical Visits

Group 1 (AM: Matsushita, PM: Sharp)

Group 2 (AM: Mitsubishi, PM: Sumitomo Electric)

8:00	Departure of bus for technical visit of Group 1
8:30	Departure of bus for technical visit of Group 2 (Incl. Luncheon)
19:00	Arrival at Kyoto Takaragaike Prince Hotel (Group 1)
17:30	Arrival at Kyoto Takaragaike Prince Hotel (Group 2)

WEDNESDAY, NOVEMBER 23RD

Excursion 1 (Nara)

8:30 ~16:30   Sightseeing Tour to Nara by bus
                 (Incl. Luncheon)

8:30   Departure from Kyoto Takaragaike Prince Hotel

16:30   Arrival at Kyoto Takaragaike Prince Hotel

16:00 ~18:00   Japanese Side Core Members Meeting
                 (Kyoto Takaragaike Prince Hotel, Room Kurama)

18:30 ~ 20:30   Reception
                 Greetings:
                     Japanese Side : Mr. Masao Teruyama, JIPDEC
                                   Mr. Yukio Honda, MITI

                     German Side   : Dr. Günter Marx, BMFT

                 (Kyoto Takaragaike Prince Hotel, Gold Room)

THURSDAY, NOVEMBER 24TH

    (1) Opening Speeches

9:30 ~ 9:40   Mr. Yukio Honda, MITI

9:40 ~ 9:50   Dr. Günter Marx, BMFT

    (2) Opening Remarks

9:50 ~ 10:00   Prof. Dr. Hisayoshi Yanai and
                    Prof. Dr. Walter L. Engl

10:00 ~ 10:30   ----- Coffee Break -----

10:30 ~ 11:15   Keynote Speech
                   "Neurocomputing"
                   (Prof. Dr. Gen Matsumoto, ETL)

11:15 ~ 12:00   Keynote Speech
                   "Integrated Optoelectronics for Communications"
                   (Dr. Claus Weyrich, Siemens)

12:00 ~ 14:00   ----- Luncheon -----

12:00 ~ 13:30   Core Members Meeting (Incl. Luncheon)

14:00 ~ 17:00   Workshops

18:30 ~ 20:30   Reception
                   Greetings:
                     Japanese Side : Prof. Dr. Hisayoshi Yanai
                     German Side   : Prof. Dr. Walter L. Engl
                   (Kyoto International Conference Hall, Swan)

FRIDAY, NOVEMBER 25TH

9:00 ~ 12:00	Workshops
12:00 ~ 13:30	----- Luncheon ----- (New Media)
12:00 ~ 14:00	----- Luncheon ----- (Computer, Semiconductor)
12:00 ~ 14:00	Chairmen's Meeting (Incl. Luncheon)
13:30 ~ 17:00	New Media Workshop
14:00 ~ 17:00	Computer Workshop Semiconductor Workshop
18:00	Transfer from Kyoto Takaragaike Prince Hotel to Rantei (Arashiyama)
19:00 ~ 21:00	Banquet in Rantei (Arashiyama)
21:00	Buses Returning to Kyoto Takaragaike Prince Hotel

SATURDAY, NOVEMBER 26TH

   (1) Summary Reports from the Workshops

9:00 ~ 9:20   Computer

9:20 ~ 9:40   New Media

9:40 ~ 10:00   Semiconductor

   (2) Closing Remarks

10:00 ~ 10:10   Prof. Dr. Walter L. Engl and
                         Prof. Dr. Hisayoshi Yanai

Excursion 2 (Kyoto)

10:30 ~ 16:10   Sightseeing Tour to Kyoto by bus
                         (Incl. Luncheon)

10:30   Departure from Kyoto International Conference Hall

16:10   Arrival at Kyoto Takaragaike Prince Hotel

II. New Media Workshop

THURSDAY, NOVEMBER 24TH (AFTERNOON)

Session 1: Broadband Network and ISDN

14:00 ~ 14:30   Concept of Packetized Video Transmission
over ATM Networks

(Prof. Dr. Y. Yasuda, Univ. of Tokyo)

14:30 ~ 15:00   Switching Concepts for Broadband ISDN

(Mr. B. Schaffer, Siemens)

15:00 ~ 15:30   ----- Coffee Break -----

15:30 ~ 16:00   ISDN in Japan

(Mr. T. Egawa, NTT)

16:00 ~ 16:30   Concept of Introduction of Boradband Communication

(Mr. V. Steiner, DBP)

16:30 ~ 17:00   Coherent Optical Techniques for TV Distribution
in Broadband Networks

(Mr. G. Heydt, HHI)

FRIDAY, NOVEMBER 25TH (MORNING)

Session 2A: Optical Switching and Optical Signal Processing

9:00 ~ 9:30   Recent Progress in Optical Switching
                  (Dr. I. Kobayashi, NTT)

9:30 ~ 10:00   Research and Development on Digital Optical
                  Processor
                  (Prof. Dr. D. Jäger, Univ. Münster)

10:00 ~ 10:30   ----- Coffee Break -----

10:30 ~ 11:00   Optical Information Processing
                  (Mr. S. Ishihara, Optoelectronics Industry and
                  Technology Development Association (OITDA))

11:00 ~ 11:30   Optical Switching, State of the Art
                  (Mr. G. Heydt, HHI)

11:30 ~ 12:00   Optical Parallel Digital Computers
                  (Prof. Dr. Y. Ichioka, Osaka Univ.)

Session 2B: Social Acceptance and Information Security

9:00 ~ 9:30   Social Acceptance and Security Problems of
                  New Information Society
                  (Mr. T. Uezono, IBM Japan)

9:30 ~ 10:00   Information Security in New Media
                  (Mr. K. D. Wolfenstetter, DBP)

10:00 ~ 10:30   ----- Coffee Break -----

10:30 ~ 11:00   Electronic Signature as an Add on to the
                  Telex Service
                  (Dr. W. Schröder, mbp)

FRIDAY, NOVEMBER 25TH (AFTERNOON)

Session 3: New Information Media Including IC Card, Optical Card and CD-I/CD-ROM

13:30 ~ 14:00   Data Broadcasting
                 (Mr. A. Yanagimachi, NHK)

14:00 ~ 14:30   Introduction of Data Broadcasting by the
                 Deutsche Bundespost
                 (Mr. K. Hummel, DBP)

14:30 ~ 15:00   Recent Progress in Optical Cards
                 (Mr. N. Gocho, Olympus Optical)

15:00 ~ 15:30   ----- Coffee Break -----

15:30 ~ 16:00   Chip Card Functionality and Applications
                 (Mr. K. Wolfenstetter, DBP)

16:00 ~ 16:30   CD-I and CD-ROM — Recent Trend in Their
                 Applications
                 (Mr. M. Horiuchi, Shingakusha)

16:30 ~ 17:00   Video Communication in the Business Field
                 (Mr. V. Steiner, DBP)

III. Computer Workshop

THURSDAY, NOVEMBER 24TH (AFTERNOON)

Session 1: Operating Systems and Real-Time Systems

14:00 ~ 14:40   Overview of the TRON Project
                      (Mr. N. Ito, Hitachi)

14:40 ~ 15:20   The BIRLIX Operating Systems
                      (Prof. Dr. G. Goos, GMD)

15:20 ~ 15:40   ----- Coffee Break -----

15:40 ~ 16:20   CTRON Research and Development
                      (Dr. F. Ishino, NTT)

16:20 ~ 17:00   X/OPEN An Open UNIX Environment
                      (Mr. Gewald, Siemens)

FRIDAY, NOVEMBER 25TH (MORNING)

Session 2: Applications of Advanced Information Technology

9:00 ~ 9:40   Electronic Patent Application System Based on
the OSI Concept

(Mr. T. Ishii, Japanese Patent Office)

9:40 ~ 10:20   Intelligent Interfaces for Knowledge based
Application Systems: The Combination of Language,
Vision and Graphics in Multimodal Systems

(Prof. Dr. W. Wahlster, Univ. Saarland)

10:20 ~ 10:40   ----- Coffee Break -----

10:40 ~ 11:20   International Online Banking Systems in Japan

(Mr. Y. Iwamaru, Mitsui Research Institute)

11:20 ~ 12:00   Benefits of Knowledge Based Techniques in
Industrial Automation

(Mr. W. Howein, Siemens)

FRIDAY, NOVEMBER 25TH (AFTERNOON)

Session 3: Highly Parallel Systems

14:00 ~ 14:40   LINKS-2: A Large Scale Multiprocessor System for
Animation

(Prof. Dr. K. Ohmura, Osakagakuin Univ.)

14:40 ~ 15:10   System Architecture for Highly Parallel Systems

(Mr. K. Solchenbach, Suprenum)

15:10 ~ 15:20   ----- Coffee Break -----

15:20 ~ 16:00   A Semantic Network Machine: IXM

(Dr. T. Higuchi, ETL)

16:00 ~ 16:30   A Parallel-Operating PROLOG Computer

(Prof. Dr. W. K. Giloi, GMD)

16:30 ~ 17:00   Computation in Neural Nets

(Prof. Dr. W. von Seelen, Univ. Mainz)

IV. Semiconductor Workshop

THURSDAY, NOVEMBER 24TH (AFTERNOON)

Session 1: mm-Wave ICs and Optical Data Links

14:00 ~ 14:40   mmICs for 30 GHz-Band Satellite Transponder
                 (Mr. H. Kato, NTT)

14:40 ~ 15:20   Development of GaAs mm-Wave ICs
                 (Dr. E. Menzel, AEG)

15:20 ~ 15:40   ----- Coffee Break -----

15:40 ~ 16:20   Millimeter-Wave Transmitter/Receivers and the
                 Devices
                 (Mr. Y. Ohgushi, NEC)

16:20 ~ 17:00   High Speed Optical Data Links
                 (Dr. R. Heidemann, SEL)

FRIDAY, NOVEMBER 25TH (MORNING), (AFTERNOON)

**Session 2: The Role of III.V. Compound Semiconductor
Devices in Future Information Systems**

9:00 ~ 9:40   The Future of Gallium Arsenide

                   (Dr. K. Shibayama and Mr. K. Fujikawa, Mitsubishi)

9:40 ~ 10:20   The Role of GaAs in Future Information Systems

                   (Dr. K. Platzöder, Siemens)

10:20 ~ 10:40   ----- Coffee Break -----

10:40 ~ 11:20   HEMT and Related New Devices Technology; Status,
Trend and Possible Impact on Future High Speed
Systems

                   (Mr. K. Dazai, Fujitsu)

**Session 3: High Speed Silicon Devices and Circuits
(including Subpicosecond Silicon Opto-
electronic Switches)**

11:20 ~ 12:00   Subpicosecond Silicon Opto-electronic Switches

                   (Mr. M. G. Lambsdorff, MPI)

12:00 ~ 14:00   ----- Luncheon -----

14:00 ~ 14:40   Silicon Bipolar Process and Device Technology
for Very High Speed LSIs

                   (Mr. T. Sakai, NTT)

14:40 ~ 15:20   High Speed Silicon Devices and Circuits

                   (Dr. A. Wieder, Siemens)

15:20 ~ 15:40   ----- Coffee Break -----

15:40 ~ 16:20   Present Status and Future Perspective of
ULSI MOS Devices

                   (Dr. E. Takeda, Hitachi)

16:20 ~ 17:00   Low Temperature Molecular Beam Epitaxy of
Silicon (Si-MBE)

                   (Dr. E. Kasper, AEG)

付録 7　企業訪問

付録 7. 企　業　訪　問

Technical Visits

Group 1:　　Matsushita Electric Industrial Co., Ltd.

　　　　　　　Central Research Laboratories

　　　　　　　Sharp Corp.

　　　　　　　Engineering Center

Group 2:　　Mitsubishi Electric Corp.

　　　　　　　LSI Research and Development Laboratory

　　　　　　　Sumitomo Electric Industries, Ltd.

　　　　　　　Itami Research Laboratories

Group 1:   Matsushita, Sharp

Tuesday, November 22nd

8:00   Departure of bus from Kyoto Takaragaike Prince
                    Hotel to Matsushita

9:30 ~ 12:00   Matsushita

                    • Main Activities on R & D

                    • Display Technologies for HDTV

12:00 ~ 13:00   Lunch at Matsushita

13:00   Departure of bus to Sharp

15:00 ~ 17:00   Sharp

                    • Main Activities on R & D

                    • Display Technologies for HDTV

                    • High Power Lasers

17:00   Departure of bus to Kyoto Takaragaike Prince Hotel

19:00   Arrival at Kyoto Takaragaike Prince Hotel

Group 2: Mitsubishi, Sumitomo

Tuesday, November 22nd

8:30   Departure of bus from Kyoto Takaragaike Prince
                        Hotel to Mitsubishi

10:00 ~ 12:00   Mitsubishi

                         • Main Activities on R & D

                         • Laser Diodes & OEIC

                         • GaAs IC

12:00 ~ 13:30   Lunch at Mitsubishi

13:30   Departure of bus to Sumitomo

14:00 ~ 16:00   Sumitomo

                         • Main Activities on R & D

                         • GaAs IC AND Material

16:00   Departure of bus to Kyoto Takaragaike Prince Hotel

17:30   Arrival at Kyoto Takaragaike Prince Hotel

List of Participants of Group 1

1.	Prof. Dr. Clemens Baack	HHI
2.	Prof. Dr. Gerhard Barth	DFKI
3.	Dr. Karin Haenelt	GMD
4.	Mr. Heydt	HHI
5.	Prof. Dr. Dieter Jäger	Univ. Münster
6.	Prof. Dr. Wolfgang A. Kaiser	Univ. of Stuttgart
7.	Dr. Eckart Raubold	GMD
8.	Dr. H. Rupf	BMFT
9.	Mr. Schaffer	Siemens
10.	Dr. Wolfgang Schröder	mbp
11.	Prof. Dr. Werner von Seelen	Univ. Mainz
12.	Mr. Struif	GMD
13.	Prof. Dr. Wolfgang Wahlster	Univ. Saarbrücken
14.	Mr. Klaus-Dieter Wolfenstetter	DBP

List of Participants of Group 2

1.	Dr. Hartmut Deyda	Embassy of F.R.G.
2.	Dr. Roland Diehl	FhG
3.	Prof. Dr. Walter L. Engl	Technology Univ. of Aachen
4.	Dr. Rolf Evers	HHI
5.	Mr. Matthias Graf Lambsdorff	MPI
6.	Dr. Wolf-Dieter Lukas	BMFT
7.	Dr. E. Menzel	AEG
8.	Dr. Karl Platzöder	Siemens
9.	Prof. Dr. Hans S. Rupprecht	FhG
10.	Mr. Karl Solchenback	Suprenum
11.	Dr. Claus Weyrich	Siemens

付録 8　参加者名簿

付録 8　参加者名簿

日本側参加者　：　59名
ドイツ側参加者　：　45名
合　　計　　104名

昭和63年度第5回日独情報技術フォーラム日本側参加者名簿

(1)　コアメンバー　　　　　　　　　　　　　　　　　　　（順不同敬称略）

議 長　柳 井 久 義　　芝浦工業大学　学長

ニューメディア

主査　大 越 孝 敬　　東京大学　工学部　教授
　　　　　　　　　　　先端科学技術研究センター　センター長
　　　戸 田　　巖　　日本電信電話株式会社　研究開発技術本部
　　　　　　　　　　　常務取締役　本部長
　　　辻 井 重 男　　東京工業大学　工学部電気電子工学科　教授
　　　沢 辺 栄 一　　日本放送協会放送技術研究所　研究主幹

コンピュータ

主査　相 磯 秀 夫　　慶応義塾大学　理工学部　教授
　　　大 野　　豊　　京都大学　工学部　名誉教授
　　　柏 木　　寛　　電子技術総合研究所　次長
　　　田 中 英 彦　　東京大学　工学部電気工学科　教授

半 導 体

主査　菅 野 卓 雄　　東京大学　工学部　教授
　　　末 松 安 晴　　東京工業大学　工学部　電子物理工学科　教授
　　　佐々木 昭 夫　　京都大学　工学部電気工学科　教授
　　　徳 山　　巍　　筑波大学　物理工学系　教授

(2) 政　　府

　　　　　本　田　幸　雄　　通商産業省機械情報産業局電子機器課　課長
　　　　　西　川　泰　蔵　　通商産業省機械情報産業局電子政策課　課長補佐

(3) 発　表　者・一般参加者等
招　待　講　演
　　　　　松　本　　　元　　電子技術総合研究所
　　　　　　　　　　　　　　超分子部　生体機能研究室　室長
ニューメディア
　　　　　寺　田　浩　詔　　大阪大学　工学部電子工学科　教授
　　　　　　　　　　　　　　（セッション 1　チェアマン）
　　　　　笠　原　正　雄　　京都工芸繊維大学　電子工学科　教授
　　　　　　　　　　　　　　（セッション 2 B　チェアマン）
　　　　　安　田　靖　彦　　東京大学　生産技術研究所　教授
　　　　　江　川　哲　明　　日本電信電話株式会社
　　　　　　　　　　　　　　NWシステム開発センター　主席技師
　　　　　小　林　郁太郎　　日本電信電話株式会社
　　　　　　　　　　　　　　交換システム研究所　研究グループリーダ
　　　　　石　原　　　聰　　㈶光産業技術振興協会　開発部長
　　　　　一　岡　芳　樹　　大阪大学　工学部　教授
　　　　　上　園　忠　弘　　日本アイ・ビー・エム株式会社　IAS担当
　　　　　柳　町　昭　夫　　日本放送協会　放送技術研究所
　　　　　　　　　　　　　　衛星方式研究部　主任研究員
　　　　　後　町　長　宏　　オリンパス光学工業株式会社　研究部　OM技術G
　　　　　　　　　　　　　　｛実際は　ドナルド・ウィリアムズ（スピーカ），
　　　　　　　　　　　　　　　堀口敏夫（技術者）の両氏が参加　　　　　　｝
　　　　　堀　内　道　夫　　株式会社新学社　電子出版事業部　常務取締役
　　　　　門　田　充　弘　　日本電信電話株式会社　担当課長

水 嶋 　 登　　日本放送協会　大阪技術部

中 村 　 孝　　日本放送協会　大阪技術部

野々村 欽 造　　松下電器産業株式会社　中央研究所　主任研究員

森 山 茂 芳　　松下電器産業株式会社

　　　　　　　　国際R&Dセンター　副参事

中 村 　 優　　株式会社東芝　総合研究所　主任研究員

正 田 耕一郎　　松下電器産業株式会社　参事

竹 内 精 一　　住友電気工業株式会社　研究開発本部　副本部長

コンピュータ

伊 藤 紀 彦　　株式会社日立製作所　武蔵工場

　　　　　　　　マイコンソフト設計部　部長

石 野 福 弥　　日本電信電話株式会社

　　　　　　　　情報通信処理研究所　所長

石 井 　 正　　特許庁　総務部電子計算機業務課

　　　　　　　　機械化企画室　室長

岩 丸 良 明　　株式会社三井銀総合研究所

　　　　　　　　総合コンサルティング部　主任研究員

樋 口 哲 也　　電子技術総合研究所　情報アーキテクチャ部

　　　　　　　　計算機構研究室　主任研究官

大 村 皓 一　　大阪学院大学　教授

河 田 　 亨　　シャープ株式会社　技術本部

　　　　　　　　コンピュータシステム研究所　所長

半 導 体

加 藤 治 彦　　日本電信電話株式会社　無線システム研究所

　　　　　　　　通信衛星技術研究部　主幹研究員

柴 山 恭 一　　三菱電機株式会社　LSI研究所　所長

太 宰 浩 一　　株式会社富士通研究所　厚木研究所　主席研究員

大 串 義 雄　　日本電気株式会社　スペース・レーザ通信事業部

レーザ・ミリ波開発部長代理

酒 井 徹 志　　日本電信電話株式会社　ＬＳＩ研究所

　　　　　　　微細加工技術研究部　部長

武 田 英 次　　株式会社日立製作所　中央研究所

　　　　　　　企画室　主任研究員

相 川 正 義　　日本電信電話株式会社

　　　　　　　関連企業本部　担当課長

豊 田 信 行　　株式会社東芝　ＵＬＳＩ研究所

赤 井 愼 一　　住友電気工業株式会社　基盤技術研究所　所長

徳 満 恒 雄　　日本電信電話株式会社

　　　　　　　関連企業本部　担当部長

(4)　事　務　局

照 山 正 夫　　財団法人日本情報処理開発協会　専務理事

山 鳥 雄 嗣　　財団法人日本情報処理開発協会　調査部　次長

兼 子 利 夫　　財団法人日本情報処理開発協会

　　　　　　　調査部国際関係チーム　主任部員

西 田 聖 道　　財団法人日本情報処理開発協会

　　　　　　　調査部国際関係チーム　主任

佐々木 真紀子　　財団法人日本情報処理開発協会

　　　　　　　調査部国際関係チーム

渡 辺 康 子　　財団法人日本情報処理開発協会　開発部

List of Participants

[Japanese Side]

1.	Dr. Masayoshi Aikawa	NTT
2.	Prof. Dr. Hideo Aiso	Keio Univ.
3.	Dr. Shin-ichi Akai	Sumitomo Electric
4.	Mr. Koichi Dazai	Fujitsu
5.	Mr. Tetsuaki Egawa	NTT
6.	Dr. Tetsuya Higuchi	ETL
7.	Mr. Toshio Horiguchi	Olympus Optical
8.	Mr. Michio Horiuchi	Shingakusha
9.	Prof. Yoshiki Ichioka	Osaka Univ.
10.	Mr. Satoshi Ishihara	OITDA
11.	Mr. Tadashi Ishii	Japanese Patent Office
12.	Dr. Fukuya Ishino	NTT
13.	Mr. Norihiko Ito	Hitachi
14.	Mr. Yoshiaki Iwamaru	Mitsui Research Institute
15.	Mr. Toshio Kaneko	JIPDEC
16.	Prof. Dr. Masao Kasahara	Kyoto Institute of Technology
17.	Dr. Hiroshi Kashiwagi	ETL
18.	Mr. Haruhiko Kato	NTT
19.	Dr. Toru Kawata	Sharp
20.	Dr. Ikutaro Kobayashi	NTT
21.	Prof. Dr. Gen Matsumoto	ETL
22.	Mr. Yukio Honda	MITI
23.	Mr. Noboru Mizushima	NHK

24.	Mr. Michihiro Monden	NTT
25.	Mr. Shigeyoshi Moriyama	Matsushita
26.	Mr. Masaru Nakamura	Toshiba
27.	Mr. Takashi Nakamura	NHK
28.	Mr. Seido Nishida	JIPDEC
29.	Mr. Taizou Nishikawa	MITI
30.	Mr. Kinzo Nonomura	Matsushita
31.	Mr. Yoshio Ohgushi	NEC
32.	Prof. Koichi Ohmura	Osakagakuin Univ.
33.	Prof. Dr. Yutaka Ohno	Koshien Univ.
34.	Prof. Dr. Takanori Okoshi	Univ. of Tokyo
35.	Prof. Dr. Akio Sasaki	Kyoto Univ.
36.	Mr. Tetsushi Sakai	NTT
37.	Ms. Makiko Sato	JIPDEC
38.	Mr. Eiichi Sawabe	NHK
39.	Dr. Koichi Shibayama	Mitsubishi
40.	Mr. Koichiro Shoda	Matsushita
41.	Prof. Dr. Yasuharu Suematsu	Tokyo Institute of Technology
42.	Prof. Dr. Takuo Sugano	Univ. of Tokyo
43.	Dr. Eiji Takeda	Hitachi
44.	Dr. Seiichi Takeuchi	Sumitomo Electric
45.	Prof. Dr. Hidehiko Tanaka	Univ. of Tokyo
46.	Prof. Hiroaki Terada	Osaka Univ.
47.	Mr. Masao Teruyama	JIPDEC
48.	Dr. Iwao Toda	NTT
49.	Mr. Tsuneo Tokumitsu	NTT
50.	Prof. Dr. Takashi Tokuyama	Univ. of Tsukuba

51.	Dr. Nobuyuki Toyoda	Toshiba
52.	Prof. Shigeo Tsujii	Tokyo Institute of Technology
53.	Mr. Tadahiro Uezono	IBM Japan
54.	Ms. Yasuko Watanabe	JIPDEC
55.	Mr. Donald Williams	Olympus Optical
56.	Mr. Yuji Yamadori	JIPDEC
57.	Mr. Akio Yanagimachi	NHK
58.	Prof. Dr. Hisayoshi Yanai	Shibaura Institute of Technology
59.	Prof. Dr. Yasuhiko Yasuda	Univ. of Tokyo

[General - Japanese Side]

1.	Mr. Toshio Kaneko	JIPDEC
2.	Prof. Dr. Gen Matsumoto	ETL
3.	Mr. Yukio Honda	MITI
4.	Mr. Seido Nishida	JIPDEC
5.	Mr. Taizou Nishikawa	MITI
6.	Ms. Makiko Sato	JIPDEC
7.	Mr. Masao Teruyama	JIPDEC
8.	Ms. Yasuko Watanabe	JIPDEC
9.	Mr. Yuji Yamadori	JIPDEC
10.	Prof. Dr. Hisayoshi Yanai	Shibaura Institute of Technology

[New Media Workshop - Japanese Side]

1. Mr. Tetsuaki Egawa   NTT
2. Mr. Toshio Horiguchi   Olympus Optical
3. Mr. Michio Horiuchi   Shingakusha
4. Prof. Yoshiki Ichioka   Osaka Univ.
5. Mr. Satoshi Ishihara   OITDA
6. Prof. Dr. Masao Kasahara   Kyoto Institute of Technology
7. Dr. Ikutaro Kobayashi   NTT
8. Mr. Noboru Mizushima   NHK
9. Mr. Michihiro Monden   NTT
10. Mr. Shigeyoshi Moriyama   Matsushita
11. Mr. Masaru Nakamura   Toshiba
12. Mr. Takashi Nakamura   NHK
13. Mr. Kinzo Nonomura   Matsushita
14. Prof. Dr. Takanori Okoshi   Univ. of Tokyo
15. Mr. Eiichi Sawabe   NHK
16. Mr. Koichiro Shoda   Matsushita
17. Dr. Seiichi Takeuchi   Sumitomo Electric
18. Prof. Hiroaki Terada   Osaka Univ.
19. Dr. Iwao Toda   NTT
20. Prof. Shigeo Tsujii   Tokyo Institute of Technology
21. Mr. Tadahiro Uezono   IBM Japan
22. Mr. Donald Williams   Olympus Optical
23. Mr. Akio Yanagimachi   NHK
24. Prof. Dr. Yasuhiko Yasuda   Univ. of Tokyo

[Computer Workshop – Japanese Side]

1.	Prof. Dr. Hideo Aiso	Keio Univ.
2.	Dr. Tetsuya Higuchi	ETL
3.	Mr. Tadashi Ishii	Japanese Patent Office
4.	Dr. Fukuya Ishino	NTT
5.	Mr. Norihiko Ito	Hitachi
6.	Mr. Yoshiaki Iwamaru	Mitsui Research Institute
7.	Dr. Hiroshi Kashiwagi	ETL
8.	Dr. Toru Kawata	Sharp
9.	Prof. Koichi Ohmura	Osakagakuin Univ.
10.	Prof. Dr. Yutaka Ohno	Koshien Univ.
11.	Prof. Dr. Hidehiko Tanaka	Univ. of Tokyo

[Semiconductor - Japanese Side]

1.	Dr. Masayoshi Aikawa	NTT
2.	Dr. Shin-ichi Akai	Sumitomo Electric
3.	Mr. Koichi Dazai	Fujitsu
4.	Mr. Haruhiko Kato	NTT
5.	Mr. Yoshio Ohgushi	NEC
6.	Mr. Tetsushi Sakai	NTT
7.	Prof. Dr. Akio Sasaki	Kyoto Univ.
8.	Dr. Kyoichi Shibayama	Mitsubishi
9.	Prof. Dr. Yasuharu Suematsu	Tokyo Institute of Technology
10.	Prof. Dr. Takuo Sugano	Univ. of Tokyo
11.	Dr. Eiji Takeda	Hitachi
12.	Mr. Tsuneo Tokumitsu	NTT
13.	Prof. Dr. Takashi Tokuyama	Univ. of Tsukuba
14.	Dr. Nobuyuki Toyoda	Toshiba

[German Side]

1.	Prof. Dr. Clemens Baack	HHI
2.	Prof. Dr. Gerhard Barth	DFKI
3.	Dr. Hans Betz	Leybold
4.	Dr. Eckart Bierdümpel	GMD
5.	Dr. Thomas Christaller	GMD
6.	Dr. Hartmut Deyda	Embassy of F.R.G.
7.	Dr. Roland Diehl	.FhG
8.	Prof. Dr. Walter L. Engl	Technology Univ. of Aachen
9.	Dr. Rolf Evers	HHI
10.	Mr. K. Gewald	Siemens
11.	Prof. Dr. Wolfgang K. Giloi	GMD
12.	Prof. Dr. Gerhard Goos	GMD
13.	Dr. Ralph Gündling	Siemens
14.	Dr. Karin Haenelt	GMD
15.	Dr. Rolf Heidemann	SEL
16.	Prof. Dr. Anton Heuberger	FhG
17.	Mr. Heydt	HHI
18.	Mr. Wolfram Howein	Siemens
19.	Mr. Klaus Hummel	DBP
20.	Prof. Dr. Dieter Jäger	Univ. Münster
21.	Prof. Dr. Wolfgang A. Kaiser	Univ. of Stuttgart
22.	Dr. Erich Kasper	AEG
23.	Mr. K.-L. Knechtel	Jessi
24.	Mr. P. Kuhn	Siemens
25.	Mr. Matthias Graf Lambsdorff	MPI

26.	Dr. Günter Marx	BMFT
27.	Mr. von Martial	NTT/GMD
28.	Dr. E. Menzel	AEG
29.	Dr. Karl Platzöder	Siemens
30.	Dr. Eckart Raubold	GMD
31.	Prof. Dr. Hans S. Rupprecht	FhG
32.	Mr. Shaffer	Siemens
33.	Dr. Wolfgang Schröder	mbp
34.	Prof. Dr. Werner von Seelen	Univ. Mainz
35.	Mr. Karl Solchenbach	Suprenum
36.	Dr. Speidel	Siemens
37.	Mr. Steiner	DBP
38.	Prof. Dr. H. Steusloff	FhG
39.	Mr. Struif	GMD
40.	Prof. Dr. Wolfgang Wahlster	Univ. Saarbrücken
41.	Dr. Ulrich Wattenberg	GMD
42.	Dr. Weidemann	Daimler Benz
43.	Dr. Claus Weyrich	Siemens
44.	Dr. Armin Wieder	Siemens
45.	Mr. Klaus-Dieter Wolfenstetter	DBP

[General — German Side]

1.	Dr. Hartmut Deyda	Embassy of F.R.G.
2.	Prof. Dr. Walter L. Engl	Techn. Univ. of Aachen
3.	Dr. Günter Marx	BMFT
4.	Dr. Claus Weyrich	Siemens

[New Media Workshop – German Side]

1.	Prof. Dr. Clemens Baack	HHI
2.	Dr. Rolf Evers	HHI
3.	Mr. Heydt	HHI
4.	Mr. Klaus Hummel	DBP
5.	Prof. Dr. Dieter Jäger	Univ. Münster
6.	Prof. Dr. Wolfgang A. Kaiser	Univ. of Stuttgart
7.	Mr. P. Kuhn	Siemens
8.	Dr. Eckart Raubold	GMD
9.	Mr. Schaffer	Siemens
10.	Dr. Wolfgang Schröder	mbp
11.	Mr. Volker Steiner	DBP
12.	Mr. Struif	GMD
13.	Mr. Klaus-Dieter Wolfenstetter	DBP

[Computer Workshop – German Side]

1.	Prof. Dr. Gerhard Barth	DFKI
2.	Dr. Eckart Bierdümpel	GMD
3.	Dr. Thomas Christaller	GMD
4.	Mr. K. Gewald	Siemens
5.	Prof. Dr. Wolfgang K. Giloi	GMD
6.	Prof. Dr. Gerhard Goos	GMD
7.	Dr. Ralph Gündling	Siemens
8.	Dr. Karin Haenelt	GMD
9.	Mr. Wolfram Howein	Siemens
10.	Mr. von Martial	NTT / GMD
11.	Prof. Dr. Werner von Seelen	Univ. Mainz
12.	Mr. Karl Solchenbach	Suprenum
13.	Dr. Speidel	Siemens
14.	Prof. Dr. H. Steusloff	FhG
15.	Prof. Dr. Wolfgang Wahlster	Univ. Saarbrücken
16.	Dr. Ulrich Wattenberg	GMD
17.	Dr. Weidemann	Daimler Benz

[Semiconductor — German Side]

1.	Dr. Hans Betz	Leybold
2.	Dr. Roland Diehl	FhG
3.	Dr. Rolf Heidemann	SEL
4.	Prof. Dr. Anton Heuberger	FhG
5.	Dr. Erich Kasper	AEG
6.	Mr. K.-L. Knechtel	Jessi
7.	Mr. Matthias Graf Lambsdorff	MPI
8.	Dr. E. Menzel	AEG
9.	Dr. Karl Platzöder	Siemens
10.	Prof. Dr. Hans S. Rupprecht	FhG
11.	Dr. Armin Wieder	Siemens

付録 9　日独情報技術フォーラム開催経緯

付録 9　日独情報技術フォーラム開催経緯

1. **第1回（日本）**

(1) 期　日　　昭和59年（1984年）4月27日（金）

(2) 場　所　　経団連会館

(3) プログラム

　午　前

　全体会議（Ⅰ）

　① 開会挨拶　　赤沢璋一　日本貿易振興会理事長

　② 来賓挨拶

　③ 議長挨拶

　　　W．エングル　アーヘン工科大学教授・同理論電気工学研究所長

　　　柳井久義　東京大学名誉教授・芝浦工業大学教授

　④ フォーラムの運営について

　　　今回の進め方，メンバー紹介

　⑤ 基調講演

　　　「日本における情報化の現状と将来展望」

　　　　　　　　　　　児玉　幸司　通商産業省機械情報産業局次長

　　　「第5世代コンピュータ技術の研究開発動向」

　　　　　　　　　　　元岡　　達　東京大学教授

　　　「ドイツ連邦共和国における情報技術の将来動向」

　　　　　　　　　U．トーマス　研究技術省第4局次長

　午　後

　テーマ別分科会（①ニューメディア②コンピュータ③半導体）

　全体会議（Ⅱ）

　① 各分科会報告

　② 総括討議

　③ 全体まとめ

④　閉　会

懇親会

2.　第2回（ドイツ連邦共和国）

(1)　期　日　　昭和60年（1985年）4月28日（日）〜30日（火）

(2)　場　所　　International Congress Center(Berlin)

(3)　総括テーマ　　Local Area Networks and Their Application

(4)　プログラム

　4／28（日）夜　レセプション

　4／29（月）

　　午　前

　　　全体会議（I）

　　　　①　開会挨拶　Dr.Probst　研究技術省政務次官

　　　　②　基調講演

　　　　　　U.トーマス　研究技術省第4局次長

　　　　　　牧野　力　通商産業省機械情報産業局電子政策課長

　　　　　　「西ドイツにおけるLANとその応用」　Prof.Dr.Baack　HHI Berlin

　　　　　　「日本におけるLANとその応用」　宮川　洋　東京大学大学教授

　　午　後

　　　テーマ別分科会（パブリックサービス，システム，コンポーネント）

　4／30（火）

　　午　前

　　　全体会議（II）

　　　　①　分科会検討結果報告

　　　　②　総括討議，まとめ

　　午　後

　　　企業訪問

　　　　・フラウンホーファ・マイクロ構造研究所

・GMD研究所

・ハインリッヒヘルツ研究所

3. 第3回（日本）

(1) 期　日　　昭和61年（1986年）10月21日（火）〜24日（金）

(2) 場　所　　京王プラザホテル

(3) プログラム

10／21（火）

午　前　企業訪問

　　〜　　┌コース①Σシステム開発本部（秋葉原），ＩＣＯＴ（三田）
　　　　　└コース②ＮＨＫ放送技術研究所（成城），光共同研究所（川崎）

午　後

夜　　ウェルカムパーティ

10／22（水）

午　前

全体会議（Ⅰ）

① 開会挨拶　　宮本四郎　日本貿易振興会副理事長

② 歓迎挨拶　　中川秀直　通商産業省政務次官

③ 基調講演

児玉幸治　通商産業省機械情報産業局長

Ｕ．トーマス　研究技術第4局次長

山本卓真　電子工業振興協会副会長

Ｎ．シペルスキー　マンネスマン・キンツレ会長

午　後

パネル・ディスカッション

テーマ：「情報技術における長期市場展望」

講　師：〔日本側〕

宮川公男　一橋大学商学部教授

小口文一　富士通㈱副社長

村松富広　日本電気㈱常務取締役

新　欣樹　通商産業省機械情報産業局電子政策課長

〔ドイツ側〕

H．J．クワイサー　マックス・プランク研究所理事

N．シペルスキー　マンネスマン・キンツレ副社長

H．シュスラー　AEGカーベル事業部長

U．トーマス　研究技術省第4局次長

夜　コアメンバー会議

10／23（木）

午　前
〜
午　後
　　　　テーマ別分科会（①ニューメディア②コンピュータ③半導体）

夜　　　バンケット

10／24（金）

午　前　　テーマ別分科会（①ニューメディア②コンピュータ③半導体）

午　後

全体会議（Ⅱ）

①　各分科会報告

②　閉会挨拶

W．L．エングル議長

U．トーマス　研究技術省第4局次長

柳井久義　議長

新　欣樹　通商産業省機械情報産業局電子政策課長

4.　第4回（ドイツ連邦共和国）

(1)　期　日　　昭和62年（1987年）10月27日（火）〜30日（金）

(2)　場　所　　The Max-Planck-Institut(stuttgart)

(3) プログラム

10／27（火）**夜**　　　歓迎レセプション

10／28（水）**午　前**　　全体会議（Ⅰ）

　　　　　　　　　　　　① 歓迎挨拶　　Lord Mayer Rommel

　　　　　　　　　　　　② 開会挨拶　　宮沢　在ドイツ日本大使

　　　　　　　　　　　　　　　　　　　Dr. Ziller，研究技術省

　　　　　　　　　　　　③ Opening Remarks

　　　　　　　　　　　　　　　　　　Engl　ドイツ側議長

　　　　　　　　　　　　　　　　　　柳井　　日本側議長

　　　　　　　　　　　　　　　　　　Thomas　研究技術省

　　　　　　　　　　　　　　　　　　新　　　通商産業省

　　　　　　　　　　　　　　　　　　　　　　電子政策課長

　　　　　　　　　　　　④ 基調講演　　Prof. Dr.　von Klitsing

　　　　　　　　　　　　　　　　　　　田中昭二教授　東京大学

　　　午　後　　テーマ別分科会（①ニューメディア②コンピュータ
　　　　　　　　　　③半導体）

　　　　夜　　レセプション

10／29（木）**午　前**

　　　　〜　　　テーマ別分科会（①ニューメディア②コンピュータ

　　　午　後　　　　　　③半導体）

10／30（金）**午　前**　　全体会議（Ⅱ）

　　　　　　　　　　　　① 各分科会報告

　　　　　　　　　　　　② Closing Remarks　柳井　　日本側議長

　　　　　　　　　　　　　　　　　　　Engl　ドイツ側議長

　　　　　　　　　　　　　　　　　　　新　　通商産業省

　　　　　　　　　　　　　　　　　　　　　　電子政策課長

　　　　　　　　　　　　　　　　　　　Thomas　研究技術省