資　料

第４回日独情報技術フォーラム
会　議　録

期　間：　昭和62年10月28日～30日

会　場：　マックス・プランク研究所
シュツットガルト

昭和63年３月

社団法人　日本電子機械工業会
社団法人　日本電子工業振興協会
日　本　貿　易　振　興　会
財団法人　日本情報処理開発協会

この資料は，日本自転車振興会から競輪収益の一部である機械工業振興資金の補助を受けて昭和６２年度に実施した「日・独フォーラム」の一環としてとりまとめたものであります。

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1．日独情報技術フォーラム趣旨

1. 日独情報技術フォーラム趣旨

日独情報技術フォーラムは，高い技術レベルと経済力を有するドイツ連邦共和国とわが国が，情報技術分野における両国の相互理解と交流を一層深め，活発な産業，技術協力の展開を通じて世界の情報化に寄与していくことを目的に１９８３年８月ドイツ連邦共和国研究技術省のリーゼン・フーバー大臣と当時の宇野通商産業大臣との間で，その設置が合意されたものである。当該フォーラムは，両国の情報技術に関わる産業分野，学術分野，および行政分野の指導的立場にある人々が一堂に会し，両国の研究開発のあり方，協力のあり方等について幅広い意見交換を行うと同時に，人的交流を深めることをねらいとしている。

当フォーラムは，毎年一回両国で交互に開かれることになっており，８４年４月には第１回が東京で，８５年４月には第２回がベルリンで，８６年１０月には第３回が東京で，それぞれ開催されている。

2．歓迎挨拶ならびに開会挨拶

2. 歓迎挨拶ならびに開会挨拶

2.1 ロンメル　シュツットガルト市長

〔歓迎挨拶〕

私は，本日，英語で皆様に御挨拶するつもりでしたが，クワイサー博士が，"それはこの町シュツットガルトおよびマックス・プランク研究所の体面上好ましくない"と考えておりまして，私も彼の考えと同じなのです。彼は私の英語のほどを知っておりますし，私も自分の話す英語をわきまえています。私にとっては，英語を使わないですむことは皆様に不快な思いを与えずにすむことで，気が安まるところです。

当研究所の理事会で私は理事長に就任しております。私の場合，専門知識がないがゆえに，皆様方の議論に何らかの邪魔をするご心配はご無用で，会議が静かにきちんと進行することを保証いたします。ある上水道事業で水槽の中の魚がもっている役目に似ている働きを，私は担っているのであります。つまり，上水道事業では魚の助けをかりて，水が健全であるかどうかのチェックをしております。研究所の教授達は，自分達のでき具合のレベルについて，私の協力によるチェックを必要としているのです。もし私が，そのでき具合を理解したと思えば，非科学的なアプローチでその出来具合が証明されたと教授達は感じるでしょう。

第4回日独情報技術フォーラムが，当地シュツットガルトで開催されますことは私共にとって真に栄誉なことであると思います。ドイツと日本の科学者達の間に緊密な協力が存続しているということを心からお慶び申し上げます。情報技術の分野で，創造性，論理的正確さ，訓練および忍耐の結合のゆえに，私共の友人である日本の皆様は，われわれにとって何か無気味な存在です。もし，皆様の日本の文字がそれほどやっかいなものでなければ，私にも皆様方がこの分野において，私共よりも数段上に位置することがわかると思います。

シュツットガルト市は，市自体で1万7千人，協力事業で8千人の職員を擁するドイツでも比較的大きな地方自治体であります。ドイツにおいても大きな組織になればなるほど，情報処理システムを導入している部門が

増加する傾向にあります。私共でも，もちろん多くの領域において情報処理システムを導入しておりますが，情報技術を含めて，多くのことが分かっていないと知られている人が先頭に立つ時，組織にとっては本質的に都合の良い場合が多いのです。それは，あたかも何でも分かっているかのように行動する人が先頭に立つよりもはるかにましなのです。しかし，何が正しいのでしょうか。人間というのは，正しいことよりも間違っていることが分かる能力を持っているものです。自然科学および工学は，この知識を利用して現在に至るまで注目すべき成功を収めてきております。われわれ政治家は，今までこの知識を十分に利用してこなかったのです。ご存知のように，真実を求める政治家は極めて少い。なぜなら，すでに真実を発見してしまったと考えているからです。彼らは，何が正しいのか理解せず，また自分のプログラムに無関係なものはすべて誤りとみなす点で，常にプログラムどおり処理しているコンピュータに似ております。世界は情報技術によって今後一層激しく変化するでしょう。人類が過去において成し遂げてきたことを，コンピュータはほとんど理解できないような速さで行います。今や，１０億分の１秒がコンピュータにとりあたりまえの時間単位です。１０億分の１秒と１秒の比較は１秒対３２年です。コンピュータは，このように１秒の中に，私が，公務員，および地方政治家としての全勤務年限の間にできるのと同じ量の仕事を処理することができるのです。私は門外漢ではありますが，今回の会議を目前にして，この学問が人類にとってきわめて責任のあることを自覚している学識経験豊かな研究者・技術者である皆様によって具体的な議論が展開されようとしており，私にとって非常に喜ばしいことであります。私はこの会議においてすばらしい進展が成され，すべての皆様がシュツットガルトで快適な滞在をされることを望みます。

2.2 宮沢　泰　在ドイツ連邦共和国大使

〔開会挨拶〕

市長，事務次官，およびフォーラム参加の皆様！　私がシュツットガルトに来ますと，いつも私は少しふるさと日本にいるような感じになるので

す。私共日本人の仕事への取組みが，ドイツの地方住民の中ではシュヴァーベン地方住民が特に勤勉であると評価されているのに似ているという関係からかも知れません。私は，第4回日独情報技術フォーラムに参加し，開会に際して皆様に挨拶を申し上げる機会を得られたことをうれしく思います。日独両国は，第2次世界大戦後の急速な経済復興を経験し，数十年来再び先進工業国に数えられるようになりました。1974年に両国は，相互の交流とより一層の協力のための基盤を，政府，学問研究，および民間企業のレベルで組織するという，科学技術協力についての協定に調印いたしました。両国の経済についての相互の影響に関する研究，および工業の分野での過去数年間の私共両国の協力関係の拡大，集約化，および凝縮化が行われてきました。具体的な例の一つは，いうまでもなくこの情報技術のフォーラムであります。すなわち，約4年前，リーゼンフーバー連邦研究技術大臣と当時の宇野通商産業大臣の協議で設立されたものであります。私共は，当初フォーラムを十分に評価できなかったというのが，私の率直な見解であります。ドイツ連邦共和国も日本も，情報技術が先端となている国の一つでありますが，それゆえに新しく獲得された知識について相互に討論することには大きな意義があり，常に新しい方向を目ざす研究作業に大いなる影響を及ぼすものです。

皆様が，このフォーラムで議論されることは，私にとっては全く分からないことだということを私は申し上げなければなりません。私は全くの門外漢であります。しかし，もし私が日々の生活やその行動から一つの判断をなすことをおゆるし頂けるならば，情報技術の分野で実現する発展進歩はまさに，驚嘆に値するものです。もちろん開発は留るものではないし，どのようにそれは進展し，私共に将来成果として何を提供することができるのか，私共は興味をそそられているといってよいでしょう。このような理由から私は，われわれ両国の間に特別に緊密な協力関係が成立していることを歓迎したいと思います。その協力が，日独の科学者や技術者達に意見交換の機会を与えるフォーラムによって，さらに強固にされるであろうことを信じて疑いません。情報技術の領域は，例えば半導体チップの開発のような基礎研究から始められ，応用研究および商品化までの，多面的な

研究および開発作業を包括しています。それゆえ，このフォーラムには様々の専門分野の専門家"研究計画を担当する専門家から著名な大学の研究者または民間企業の人々まで"が参加しています。われわれはこのシュツットガルトでのフォーラムから貴重な成果が得られることを期待しております。

終わりに，約2週間ほど前に知らされた今年のノーベル賞受賞者に対して一言申し上げさせて下さい。ノーベル物理学賞を受賞された，ベトノルツ博士に心からお祝いを申し上げます。超電導物質についての彼の発見は，情報技術の分野でも影響を与えるにちがいありません。一方，日本人の生理学者である利根川博士が，今年ノーベル医学賞を受賞されたことについても喜びを申し上げたいと思います。しかし，このフォーラムの最も重要な参加者の一人である田中昭二博士の研究にも言及しなければなりますまい。今年のベトノルツ博士受賞の前提条件を，田中昭二博士の研究が成し遂げたのであります。私の挨拶を次のような期待をもちつつ終えたいと思います。すなわち，このフォーラムが多くの成功を遂げ，情報技術の分野での業績が持続して実り豊かであるように。ご清聴を感謝します。

2.3 ツィラー　研究技術省事務次官

〔開会挨拶〕

敬愛なる大使，市長，皆様！　この日独情報技術フォーラムが，今日この地，固体研究のためのマックス・プランク研究所で開催される運びとなったことは，私にとって特別な喜びであります。また，情報技術の専門家でもない私が，この演壇に立つことに配慮をして下さり大変感謝しております。私は，この会議の準備に際して示された研究所の全職員のご支援に対して，また，この研究所のわれわれへのもてなしの素晴しさに対して，心から感謝を申し上げます。この固体研究を中心としたマックス・プランク研究所は，１９６９年の創立以来，内外の科学者の出会いの場所として発展してきました。日本からの客員研究者は，ご存知のように，この研究所ではよく見受けられます。そのことに対し，政府は所長に深く感謝するものであります。私は，当地シュツットガルトでこのフォーラム

が行われるような，自由な意見の交換の特別の意義について考えてみたいと思います。学問というものは，少し古風な表現を用いるならば，第一に静かで小さな研究室での研究によって生きるものであり，第二にそれは，固有の成果を吟味することおよび実り豊かにするために，他の研究者との討論および意見の交換を必要不可欠なものとしております。孤立は害になります。なぜなら，孤立は学問の分野を複雑なまま把握することにより，難しくするからです。情報技術を専門に扱う皆様方は，そのことをご存知でありましょう。このように，基礎研究での国際的な協力が自明のことになっているにもかかわらず，私共は，時々産業面での研究および開発における国際的な協力を，とても難しく扱っている場合があると思います。確かに，これは理解できる面もあります。すなわち，産業的な研究および開発は，新しい知識によって世界市場における競争力の優位性を獲得するという目標をもっているからです。将来のために企業は投資するものです。そして，この点から特別の研究成果についての秘密保持，および外国のパートナーとの協力によって，相互の利益を最大限に増やすという期待が結果として生まれてきます。こうした点を解決することが重要であります。電界の両極と同様こうした利害の衝突が，国際的な分野にもあり，この衝突は国内と同じように国境を越えようとするのです。ご承知のとおり，安定した世界経済はオープンな経済関係に依存しております。このことは，国際的な分業と国際間の知的伝達にも依存しているのです。閉ざされた門戸の中では，進歩も発展もないでしょう。ドイツ連邦共和国と日本は，輸出経済の大国，高度な技術を所有した国であり，開かれた世界市場と自由な知的伝達に寄与するためにも，政府としては垣根を取り払い，研究者同士また，経済上の競争者同士の対話を国家の枠を超えて促進する事が重要だと思っています。この精神にのっとって，１９７４年以来，大使が既に言及された日独政府間の協定があるのです。連邦政府もまた，この協定にそって発展してきた協力は非常に成功したと考えており，さらにこの協定は今後の進展のための良き契機となるものと考えております。例えば，喜ばしいことに，１９８８年には日本にドイツ研究所が設立されるのは間違いないということです。しかし，この研究所は情報技術に携るのではなく，

精神科学と社会科学の非常に重要な領域の仕事を致します。有難いことに，この研究所設立にあたっては，マックス・プランク協会のご協力を頂きました。

情報技術は研究だけでなく経済面にも関わる，難しく微妙な領域です。それというのは，今日では純粋に科学技術的な問題だとは見なされなくなっているからです。非常に顕著な経済的な利害がからみ，かつ私共の生活と仕事の世界に重要で決定的な影響を与えております。実際，政治のほとんどすべての分野にも入り込んでいます。この情報技術については，連邦政府がすでに１９８４年3月，政府報告で，この技術の挑戦を受けるべきだという決着をまとめております。さて私は，昨晩の会話を取り上げることにしましょう。今われわれが議論しているのは，宇宙空間の研究における実行と予算の諸問題です。しかし，連邦政府がそういった種類のプロジェクトだからという理由で，情報技術促進のための支出を，差し控えるのではないかと心配する必要はありません。宇宙空間についての研究テーマの分類方法が難しいために，研究技術大臣は，基礎研究，予備研究とその他の重要な領域（情報技術もその１つなのですが）に，区分けをするような事になってはいけないと強調しておきたいわけです。連邦政府首相は，その所信表明演説の中で，さらに歩をすすめた情報技術のコンセプトを公けにしました。このコンセプトが現在のところ，検討されております。このコンセプトは，ドイツ連邦共和国内の状況，西暦２０００年までの情報技術の将来の発展，ドイツ連邦共和国によって準備された，より良き枠組のための条件を創り出す基準を明らかにし，さらにドイツ人の研究とドイツ人の経済のために新しい刺激を与えることになるでしょう。そして，この関係では当然のことながら，科学技術の分野における協力の問題が，ヨーロッパの枠内のみならず大陸間という枠内でも重要な役割を演ずることになるでしょう。他方，私共が既に地球的な共同体の使命だと考えた様々なテーマ，例えば，環境，癌，エイズ，原子炉の安全性，地球自身の研究，気象，天文学，第三世界に対する農業研究等々については，世界市場でおたがいが競争している領域については困難であるとしても，このフォーラムの終りに将来の協力のための基準目録ができれば幸いだと思います。し

かし，もしこれが不可能としてもこのシュツットガルトでのフォーラムにおいて，一緒になってただ本音を吐くというにとどまらず，相互信頼を打ち建て，基礎的領域でもあるいは産業の領域でももっと集中的な科学技術上の協力のための関係を１つでも２つでも創り出すべく寄与できるのではないかと思います。そして，もし，これがうまく行ったら，このフォーラムに両者が参加したかいがあったというものです。それゆえ，主催者，この会議の議長，産業界とか学術分野から来ていただいた方々によろしくお願い申し上げます。こうした方々のご努力があって，ようやくただいま始まりました行事が意義あるものになると思います。どうかこの３日間，同フォーラムの参加各位は，できるだけ多くの有意義な印象を得られ，ここで得た友好関係をフォーラム終了後も両国のために継続することをお願い致します。この行事が成功裏に幕を閉じることを祈り，…私は，シュツットガルトの古い人間として，実際本日の役目柄，申し上げてよいかと思いますが…土地の守護神が，必ずや多大な力を貸して下さる事と存じます。ご清聴ありがとうございました。

2.4　W. L. エングル　　ドイツ側議長　アーヘン工科大学教授

〔開会挨拶〕

大使閣下，皆様！　第４回日独フォーラムの開催にあたり，皆様をお迎えできたいへんうれしく思います。今回，日本とドイツ両国の科学関係において長い歴史を持つ都市でお会いできました。私たちのためにご協力を賜わったマックス・プランク研究所，とくにこの催しを企画するに当たり，たいへんご努力なさったクワイサー博士とそのスタッフの方々に感謝いたします。

世界情勢は，経済上の成功や失敗によるばかりではなく，緊迫が増しているのが特徴になってきています。このようなときに，ここに科学のアイデアを交換できる機会をつくってくださった政府に尊敬の念を払いつつ感謝いたします。

今朝，ここで皆様ご存じの田中昭二博士とクラウス・フォン・クリッツィング博士のお話しをいただけることはたいへん光栄です。

皆様方が共通の理解の下にディスカッションなさることを期待いたします。「友，遠方より来る，また楽しからずや」の言葉のように，ご一緒に楽しんでください。

ありがとうございました。

2.5 柳 井 久 義　　日本側議長　芝浦工業大学学長

〔開会挨拶〕

ただいまドイツ側の議長のエングル先生から日本語でごあいさつがございました。私は本当はドイツ語でやるべきかもしれませんが，昨晩，つたないドイツ語でやりましたので，本日は日本語でやらせていただきます。

ただいまエングル先生から，素晴らしいイントロダクションのお話がございました。私といたしましても同様の感じでございまして，今回，このシュツットガルトの地で第4回フォーラムを開催できたことをたいへんうれしく存じております。

このフォーラムは，いままでもそうでございましたが，今後の日独情報技術関係における友情と交流を深め合うためのものでございまして，今回のフォーラムそのものが，おそらく皆様の積極的なご参加によりまして成功裏にその実が上がるものだろうと思っております。今回の成果をさらに将来とも発展させていきたいと思いますので，皆様のご協力を深くお願い申し上げるところでございます。

簡単でございますが，開会のごあいさつに代えさせていただきます。ありがとうございました。

2.6 U. トーマス　　研究技術省第4局次長

〔開会挨拶〕

大使様，市長様，州政府事務次官様，議長様，日本のゲストの皆様，そして本日お越しの皆様！　私共は，昨年このフォーラムのドイツ側のコアメンバーの皆様と検討した結果，今回のフォーラム開催を当地に決定しました。私共の日本からの友人の皆さんは，すぐにシュヴァーベン人は日本人によく似ていると思われることでしょう。非常に愛すべき人達ですし，

かつまた非常に危険な競争相手でもあるのです。私共連邦政府内では自ら経験した事ですから，これについては良く存じているのです。といいますのは，州政府と連邦政府は，実際非常に手強い競争相手であります。この美しい研究所を第4回のフォーラムに供して頂き，まことに有難く存じます。

ここでは，将来のためにただ2つのことを申し上げたいと思います。一つは，昨日，一昨日と，通商産業省の新電子政策課長と私共とで話を致しまして，意見が一致した点があります。それは情報技術の分野で，独日の科学者の協力が，年々非常に良くなってきたという事です。また，こう言ってよければ，この分野で問題が起こっても，両国の関係官庁はいつでも，力を貸せる所では力を貸し，問題を解決する用意があるという点でも意見が一致しました。といいますのは，大学の付属機関と専門の研究機関の間のコンタクトを深めるのが私共の目標だからですし，これができるのは，定期的に会い，若い人達にもその都度色々な州に来てそこで一緒に仕事ができ，新しい事に触れ，友情を結び，それが将来も続く，といったことからです。そういう訳で，できるだけこれらの出会いの場があればと思っています。

第二は，このフォーラムは3年前に，リーゼンフーバー大臣と宇野大臣によって決定されたものですが，両国の産業分野，技術分野からの著名な代表者同士の非公式の出会いの場であるという意義があります。この与えられた機会の真価をよく理解される事を切に願う次第です。そして，両国のためにつまり科学者・技術者同士の出会いとまた産業分野・学術分野の代表者同士の出会いのために，私共は自ら音頭をとらせていただきます。私共は場所を提供すると同時に，皆様方に様々な可能性を提供したいと思っていますが，これを生かすのは皆様方にかかっています。この意味で，私自身がこのフォーラムの将来のためにも様々な準備をしなければならないと思います。ありがとうございました。

2.7 新　欣樹　通商産業省機械情報産業局電子政策課長

〔開会挨拶〕

市長閣下，大使閣下，次官そしてご列席の皆様！　本日，ここに第４回日独フォーラムが開催されるに当たりまして，通商産業省を代表いたしまして，一言ごあいさつ申し上げます。

まず，エングル先生，柳井先生の両議長をはじめ西ドイツ研究技術省，ＧＭＤ，また日本側のＪＥＴＲＯ，ＪＩＰＤＥＣ，さらには開催地でございますバーデンビュルテンベルク州シュツットガルト市，マックス・プランク研究所等の各位が，当フォーラムの開催に向け寄せられましたご努力に対し，深甚なる敬意を表するしだいであります。

日独情報技術フォーラムは，高い技術レベルと経済力を有するドイツ連邦共和国とわが国が，情報技術分野における両国の相互理解と交流を一層深め，活発な産業技術協力の展開を通じて世界の情報化に寄与していくことを目的に，１９８３年に研究技術省と当省との間の合意に基づき設置されたものであります。

以来，両国の情報技術にかかわる産業分野，学術分野および行政分野の指導的立場にある人々が年１回，一堂に会し，幅広い意見交換を行うとともに，人的交流が深められてまいりました。

今回はＨＤＴＶ，ソフトウェアエンジニアリング，超電導などといったニューメディア，コンピュータ，半導体の各分野におけるホットなテーマに関し，両国の第一線の研究者から研究成果の発表が予定されております。日独両国に，世界の繁栄に対する創造的な貢献がいままで以上に期待されている今日，創造的科学技術の分野で世界に冠たるマックス・プランク研究所においてこのようなフォーラムを開催できることは，まことに時と所を得たものと考えるしだいであります。

１週間ほど前に起こった株価の大暴落は，世界を震憾させましたけれども，同時に世界の経済活動がいかに密接に関連し合っているかということを改めて思い起こさせました。

情報技術の目覚ましい発展を背景に，現在，地球的な規模で情報化が着実に進みつつあります。また，情報化は国境を超えた情報の流通を促し，

各国経済社会の国際化にも重要な役割を果たすものと期待されております。

そのようななかにあって，日独両国が情報技術分野における交流を通じ，世界の情報化，ひいては世界経済の活性化に貢献できることを期待してやみません。

最後に，本フォーラムが，皆様方の活発な意見交換を通じて成功裏に進められますこと，および本フォーラムが今後とも一層発展いたしますことを祈念いたしまして，私のごあいさつとさせていただきます。ありがとうございました。

3. 各分科会サマリー

3. 各分科会サマリー

3.1 ニューメディア分科会

〔ニューメディア分科会ドイツ側主査　C. Baack〕

お早うございます。ニューメディア分科会で話し合った内容のサマリーを発表したいと思います。

ニューメディア分科会は，２日間にわたり高品位テレビ（ＨＤＴＶ）についての様々な問題について話し合いました。ＨＤＴＶは，視聴者に，できるだけ本物に近い自然な映像を提供することを目的としています。日本では，ＨＤＴＶ技術は２０年前から研究されてきました。ドイツのHDTV研究は，研究技術省の奨励下で７０年代後半に始まりました。

日本以外では，ＨＤＴＶの研究活動は，そのほとんどがドイツで実施されていると言わなければなりません。将来家庭で利用されるHDTVディスプレイがＨＤＴＶの主要機器であるため，最初のセッションではＨＤＴＶディスプレイ技術，フラットパネル，プロジェクション型デスプレイに焦点をあて，関連テーマについて話し合いました。

シュツットガルト大学のLüder教授が，薄膜トランジスタを採用したアクティブ・マトリックス技術の研究結果を発表しました。彼は，シュツットガルトで考案されたセレン化カドミウムプロセスに利用されているＴＦＴ技術について詳しく説明しました。

ＮＨＫの平島氏が現在最高のフラットパネル技術の研究および比較結果を発表しました。ＮＨＫのプラズマ・ディスプレイ・パネルと，２０インチ・ディスプレイの最近の成果が報告されました。

ヘキスト社（フランクフルト）のFelcht博士も，強誘電体ＬＴＤに重点を置きながら，液晶材料の諸問題について発表しました。

松下電器の野々村氏は，フラット・カソードレイチューブ・パネルに対する様々な既知のアプローチに関する研究結果を紹介しました。松下電器が開発した自給構造を持つマトリックス駆動フラットＣＲＴが詳しく説明されました。

最後に，ＨＨＩのGerhard-Multhaupt博士が，ソリッドステートのライ

トバルブについて詳しい紹介しながら，ハイライト出力大型スクリーン・プロジェクションを行うためのライトバルブ・アプローチの研究内容を発表しました。

総合的に，ＣＲＴとソリッドステートのライトバルブのプロジェクションが，将来２メートルのデスプレイを実現するためのコンパクト・プロジェクターとして有力候補であると考えられることが明らかになりました。ずっと先の将来には，プラズマ・ディスプレイとフラットＣＲＴが，大型ＨＤＴＶディスプレイのための最有力候補と考えられます。

ニューメディア分科会の第二セッションでは，ＨＤＴＶスタジオと消費者の間に必要となるトランスミッション・リンクについて論じられました。ＮＴＴの三木氏が，現在日本で開発中のＨＤＴＶ帯域圧縮コーディング技術と広域通信システム技術について紹介しました。帯域圧縮コーディングとして，彼は，２種類のアナログ・フォーマット・コーディング・スキームと，ビット速度が１４０メガビット／秒以下のデジタル・コーディングを紹介しました。

広域通信システムについては，ファイバーオプティック技術を使ったコスト効果の高いローカル・ディストリビューション・ネットワーク・アーキテクチャの重要性が強調されました。光周波数分割マルチプレックス・リンクへの好調な傾向が有力であることも紹介されました。ドイツ郵政省の研究所の Stenger 博士は，より一般的なＨＤＴＶ通信の問題について話されました。

例えば，衛星，ＣＡＴＶ，広域ＩＳＤＮおよびユニバーサル広域ネットワークなどの通信メディアについて紹介しました。また，ＶＩＷＥＳ，高解像度ＭＡＣ，デジタル広域通信フォーマットなどの通信フォーマットについても説明されました。さらに，互換性，非互換性に関する今後の戦略についても説明しました。近い将来のＨＤＴＶ通信の可能性については，ヨーロッパでは衛星通信ですが，ベルリンのＨＨＩが行っているコヒーレント光通信システムの優れた研究から，大いに有望視されています。

全般的に，このような長期展望の分野では，日本とドイツの見解は非常に似ていると思われます。これは，将来の対話と協力関係にとって非常に

望ましい基盤となります。

ニューメディア・グループの第三セッションでは，ＨＤＴＶレコーダーやＨＤＴＶカメラなどのスタジオ設備が話し合われました。ソニーの橋本氏が，ソニーのデジタルＨＤＴＶレコーダーについて，設計上の重要な問題やこれまでに達成された成果をまじえながら，詳しく説明しました。テープ・ヘッド・コンタクトとイコライジング・シミュレーションが紹介されました。Broadcast Television Systems のHausdörter博士が，ピックアップ・チューブとソリッドステート・イメージャーの長所，短所を考察しました。現在のソリッドステート・イメージャーは，低感度という欠点がありますが，ノイズ比の向上を導きます。これは，将来のＨＤＴＶのアプリケーションにとって好都合であると思われます。

会議では，値段はチューブとは比べられないだろうというコメントが出されました。

池上通信機の堀氏が，３０㎜の planned ikon を採用した池上通信機の新しいＨＤＴＶカメラのコンセプトについて説明しました。従来の satikon を使ったカメラとの性能比較を行い，周期ノイズ比は高いが，lack が低いことを発表しました。このカメラは非常にコンパクトで，間もなく市場に出ると思われます。

さて，高品位テレビは，本当の情景を自然な映像として映す試みへの非常に重要な一歩です。しかし，自然に近い映像を映すという試みの最終段階は，当然，三次元テレビでなければなりません。ですから，私たちのシンポジウムの最後のセッションでは，三次元テレビについての討論が行われました。

東京大学の浜崎教授が，レンズ・プレートと特殊なビーム・インデックスＣＲＴを組み合わせて作った自動立体三次元画像を紹介しました。利用された方法と，インデックス回路構造が詳しく説明されました。ここでは，デスプレイ面積２２センチ×２８センチが紹介されました。

ＨＨＩの Börner氏が，レンズ状のスクリーンを使った大型デスプレイの三次元テレビについて説明しました。対角線の長さ2.5メートルの三次元画面は，眼鏡を使わなくても見ることができます。この原理が詳しく説明

された後で，スクリーンの設計について討論が行われました。また，６台のＴＶカメラと６つのＣＲＴプロジェクター装置の説明も行われました。紹介された２つの方法は，アプリケーション分野が全く異なることが，討論で指摘されました。娯楽用として，大型画面が必要とされていると考えられました。

以上，４つのセッションで詳しく討議されましたテーマをまとめて報告しました。最後に，各講演は素晴らしく，非常に優れた研究結果が紹介され，実り多く率直な討論が行われたということを申し上げたいと思います。どうもありがとうございました。

3.2　コンピュータ分科会

〔コンピュータ分科会ドイツ側主査　G. Goos〕

コンピュータ分科会からご報告します。後半は相磯教授から報告していただきます。

コンピュータ分科会には，日本から９人，ドイツから１３人の計２２人が出席しました。日独の大学から２件，公的研究機関から５件，産業界から７件の計１４の論文発表が行われました。

３つのセッションでは，「フォールトレランス・システム」「ソフトウェア・エンジニアリングの方法論」および「ソフトウェア・エンジニアリング環境」のテーマが取り上げられました。これらのテーマは，日独が何回かのやりとりの上で合意したものです。まとめますと，フォールトレランス・システムの発表では，研究開発段階から実際のアプリケーションまでの推移が詳しく説明されました。

このセッションは，生物システムに類似するアプローチを紹介した井原氏の講演が目を引きました。ソフトウェア・エンジニアリングの方法論と環境についてのセッションでは，産業界と学術界の両方の視点でこれらのテーマが論じられました。実用化が間近のものもありましたが，これから１０年間に解決しなければならない問題も多く残されていると思われます。

ここで，ドイツ側の論文発表について報告します。日本側の分については，相磯教授から紹介されます。

フォールトレランス・システムのセッションでは，Braunschweig 大学の Leilich 教授によるデータベース・マシーンと宇宙実験のハードウェアの紹介から始まり，全般的には，特殊ハードウェアは，汎用システムと競合できないことが多いということが指摘されました。特殊ハードウェアは，余りにも特殊すぎてフレキシビリティに欠け，値段が高く複雑すぎるという欠点があります。技術進歩が急激で，次世代の汎用システムが余りにも早く出現してしまうので，経済的に生き残れる製品を開発する時間的余裕がありません。

Leilich 教授は，コンポーネントやシステム・レベルでのフォールトレランスの要件について説明しました。これは，彼のグループが，衛星や惑星間ロケットに組み込まれた計算装置の設計時の実際に満たした要件です。非常に厳しい要件ですが，決して適合不可能なものではなく，基本的にはハードウェア・アプローチです。この点については，ソフトウェアの問題はそれほど重要ではありません。

Krupp Atlas Elektronik の Meyerhoff 博士は，デュプリケート・マルチプロセッサ・システムに基づくフォールトレランス・プロセス制御システムを紹介しました。この２つのシステムは，完全に同期化して並行に作動します。使用中のシステムに故障が発見されると，ただちにスタンバイ・システムが代わって作動します。同期化機能と比較機能は，マイクロ・コード化された命令によって実行されます。このシステムは，オペレーショナル・システムで，多くの装置で完全なトレランスを持つことが試験で立証されています。

第一セッションの最後は，ＧＭＤベルリンの Behr 博士の発表が行われました。オープン従属型分散型コンピュータ・システムのアーキテクチャについて，欧州の研究プロジェクトＤＥＬＴＡ４を紹介しました。このプロジェクトの目的は，日立の井原氏が発表した自動分散型システムと非常によく似ています。最大の違いは，欧州が異質のホストを持つオープン環境に向かっているのに対し，日本は，閉鎖型コミュニケーション・システムをもつ同質ステーションを目標に開発しています。

ＤＥＬＴＡ４システムは，複製ソフトウェア・コンポーネント間でメッ

セージの伝送を行う信頼性の高い通信システムを基礎にして，さらに開発が進められています。この通信システムは完全な分散型です。ソフトウェア環境のアプリケーションは，オブジェクト指向の機構に基づいています。

ソフトウェア・エンジニアリングの方法論に関するセッションでは，ドイツ側が2人，日本側が2人の論文発表が行われ，アプローチごとに2つに分けて発表しました。

SiemensのHowein氏が，産業用オートメーション・ソフトウェア専用のソフトウェア・ファクトリーへのアプローチについて発表し，方法，ツール，組織が成功を導く3つの鍵であると述べました。また，強力なワークステーション・ネットワークの上に築かれたワークベンチ，要件分析を設計するための総合的ツール，グラフィック・ユーザー・インタフェースに基づくユーザー・フレンドリ性，基準および品質保証の尺度を，より方法論的な観点から考察しました。井原氏は，新たな開発では年間8％，コンポーネントの再利用では16％も生産性が伸びたと述べました。これは，非常に驚異的な成果であり，これまで，このような高い数字を達成した例はほとんどありません。ですから，これは非常に興味深い発表であると同時に，あとでかなりの論議も呼びました。最後の発表者のHowein氏から，今後は，情報をベースにしたツールから発展が見られるであろうという予測が述べられました。

カールスルーエのFraunhofer GesellshaftのSteusloff教授は，ソフトウェア・エンジニアリングのための集積ツール・セットへの総合的なアプローチに関する講演を行い，ツール集積化の一般的な問題について論じ，ユーザー・インタフェース，ツール，データ操作およびデータベース間のインターフェースを標準化することの重要性を強調しました。BMFTが後援するユニバーサル・プロジェクトについて説明しました。

全体を要約すると，ソフトウェア・エンジニアリングの問題を解決するための，ユニークかつ明快で一般に認められる総合的方法論が生まれる兆しはみえていません。現実的には，これから実現される理想のものではなく，現在すでに利用できるものを使わなければなりません。これによって，ある程度の生産性の向上はもたらされましたが，問題の最終解決はまだ先

です。しかしながら，ほとんどの参加者は，１９９０年代にはいくつかの新しい方法論が導入され，最終的に，ソフトウェア構築のための非常に有用な数学的アプローチとして結実するであろうという松本氏の意見に同意しました。このようなアプローチについては，多くの重要な点について，まだ基礎研究すら行われていません。また，実際に利用した段階で，さらに深刻な教育的問題が提起されると思われます。

ソフトウェア環境に関する最終セッションは，Hruschka博士の論文で始まりました。博士は，コンピュータを利用した総合ツール・システムについて発表しましたが，これは，所属しているＧＥＩの社内要件から導いたもので，基本的にはリアルタイム・アプリケーション向けのものです。フレームワークの側面も広く利用されて，他の外部のツールに対するオープン・インタフェースも利用できます。各国では，市場に出ている製品を利用することができます。

カールスルーエの情報研究センターのDittrich博士は，ボトム・アップ・アプローチとして，集積ツール・セットのニーズを満たし，ユーザが必要とする効率を満足する目的指向型データベース・システムについて発表しました。これは，現在建設中であり，実用性についての試験が行われています。

このセッションの最後に，ミュンヘンのSoftlab社のAbbenhardt氏が発表しました。彼は，産業化されたアプローチに近いソフトウェア開発プロセスを生み出す遠大なコンセプトであるとして，欧州のEureka Projectを紹介しました。現在は目標と戦略を定義するための定義段階で，あまり詳細には進んでいません。

総合的に，ツールのブラックボックス・インテグレーションとオープン総合ツール・セットに関するフレームワーク・アプローチは，現時点では，特殊な性質と利点があるという結論に達しました。ブラックボックス・システムは製品として入手できますが，特定の環境だけに限定されています。オープン・システムは，今でも，多くの問題を抱えていますが，ユーザのニーズに合わせた特殊なシステムを作る機会があれば，より一層利用機会が増えるでしょう。ソフトウェア・ファクトリーのアプローチは，将来的

には，オープン・インテグレーテッド・ツール・セットの能力を強化することになるでしょう。これで，私の担当するサマリーの発表を終わります。相磯教授お願いします。

〔コンピュータ分科会日本側主査　相磯秀夫〕

皆様お早うございます。日本側のコンピュータ分科会による発表をまとめたいと思います。フォールトレランス・システムと題した第一セッションでは，東京工業大学教授であり，日本のフォールトレランス・コンピューティングに関する研究グループの会長をつとめる当麻教授が，最近，大学や研究所を中心に進められているフォールトレランス・コンピューティングについてのいくつかの研究テーマを紹介しました。

セルフチェック回路，テスト可能な設計，人工知能，または論理的言語PROLOGを使ったテスト生成プログラムへの知識アプローチ，マジョリティ・ボードなどのフェイル・ソフト・システムの理論を紹介しました。ソフトウェア・エンジニアリングに関係するフォールトレランス・コンピューティングや，フォールトレランス・システムの実用化や産業開発については，発表時間が短かったためにあまり詳しく触れませんでした。

日立の井原氏は，フォールトレランス計算技術を大規模なリアルタイム・システムに応用したケース・スタディについて発表しました。このシステムは，多くの例で，フォールトレランスの拡張性と保全性が要求されます。システムが上記の条件を満たせるように，生物的アナロジーに基づく自動分散型制御システムに対する新しい設計コンセプトが提案されました。

その他にも，このようなフォールトレランスの自動分散型システムを実現する上で重要な技術的問題についても発表しました。設計コンセプトの効果が正しいことを立証するために，ファクトリー・オートメーションの制御や鉄鋼生産工程制御システムへのアプリケーション・システムの可能性についても説明しました。

ソフトウェアの方法論と題した第二セッションでは，ＮＴＴの花田氏が，ソフトウェア生産自動化の研究についてその概要を紹介しました。彼は，この研究を「定理の証明」「事例からの合成」「高水準記述からの合成」

および「プログラム要素の再利用」の４種類に分類しています。また，２種類の合成方法を例にとって説明しました。ひとつは，自然言語に基づくソフトウェア開発システムで，もうひとつは，システム記述環境です。後者は，サービス要求の高まりに対処するために通信ソフトウェアを効果的に実行するための環境です。

ソフトウェア需要の拡張，低いソフトウェア生産性および専門のソフトウェア・エンジニア不足などが原因で，現在の情報技術のあらゆる層で発生しているようにみえる重大なソフトウェア危機を回避するために，日本電気の松本氏は，ビジュアライゼーションの自動化とソフトウェアを利用することを提案しました。このコンセプトの一例として，日本電気で開発され，様々な場所で利用されているソフトウェア・エンジニアリング・アーキテクチャを説明しました。このシステムの最大の特徴は，設計と生産の質の向上，プログラムの読みやすさ，高品質プログラムのテストと設置の生産性の向上を保証することです。

ソフトウェア・エンジニアリング環境と題した第三セッションでは，情報処理振興事業協会のシグマ・プロジェクトの秋間氏が，世界的に注目されているシグマ・プロジェクトについて紹介しました。これは，通商産業省から研究奨励金が出ているソフトウェア開発技術の推進プロジェクトです。彼は，このプロジェクトの背景，目的，特徴，シグマ・システムのフレームワーク，システム構成，データベースとネットワーク・サービスおよびシグマ・ワークステーションとオペレーティング・システムのプロトタイプおよび将来の展望について詳しく説明しました。

シグマ・ワークステーションの重要な特徴のひとつとして，第三セッションではマルチメディア・ウィンド・システムを詳しく説明しました。彼は，機能要件の設計ポリシー，ハードウェア要件，マルチメディア・ウィンドウとプリンタなどの設備，ソフトウェア製造プロセスについて紹介しました。このプロジェクトは，ソフトウェアの生産性が向上し，ソフトウェアの信頼性と質を高めることが予想されるため，国際的に広く注目されています。

最後に，コンピュータ分科会のセッションについて総合的なコメントを

述べたいと思います。このフォーラムは非常に有意義で，両国の優れた研究者との意見交換を楽しみました。このフォーラムは将来も討論を続け，協力しあう価値があると思っています。しかしながら，もう少し発表件数を減らすべきだったと考えています。最近の技術的テーマを話し合うには発表件数が多すぎて，限られた時間が無駄に使われてしまいました。これは，前回のフォーラムでも指摘されたことですが，まだ改善されていません。ですから，日本で開かれる次回のフォーラムでは，構成内容を変えることを提案したいと思います。

実用的なフォールトレランス・コンピューティング・システムに関するドイツ側からの発表については，日本よりずっと多くのシステムの研究が進められているという感想を持ちました。また，ソフトウェア・エンジニアリング環境の開発に関する実際の研究方法に，非常に強い感銘を受けました。これは，製品の効果を立証できたと考えています。

これで発表を終わります。どうもありがとうございました。

3.3 半導体分科会

〔半導体分科会ドイツ側主査　H. J. Queisser〕

共同主査の田中昭二教授に代わりまして，半導体に関する討議結果を発発します。非常に素晴らしい会議であり，特に，構成が適切であったと思います。また，発表原稿数も適切であり，コンピュータ分科会のように時間の配分を気にする必要もあまりなく，次々と発表が進みました。

半導体は，当然のことながら，優れた材料であり，この材料を支配するものは情報技術を支配します。ですから，半導体の討議には所有権が主張される問題が多く含まれていますが，このような微妙な分野にはふれずに進めました。私たちは，競争が行われる前の分野，特に，材料指向型の研究開発と，その分析，製造方法についての見解や研究結果の交換を中心に討論を進めました。

しかしながら，種々の分野における将来のデバイス製造の見通しは非常に明るいと感じました。例えば，桜井氏は，オプトエレクトロニクス集積

回路トランスミッターのスライドを見せてくれました。このスライドは，近い将来に登場するものを暗示しています。彼の講演では，この回路の心臓部となるアルミニウム砒素，ガリウム砒素のレーザー・エミッターが主テーマとして取り上げられました。また，これに関与する開発，材料および加工技術を紹介しました。

アカデミックな側面からの見解として，Pilkuhn 教授が，von Klitzing 教授がオープニング・セッションで述べた内容の延長ともいえる非常に素晴らしい発表を行いました。これは，バンド構造エンジニアリングの総合的な概念で，特定の光放出装置，レーザーなどにとって望ましく，必要な電導性や不連続な価電子帯を作るためのものです。素晴らしい発達を遂げている非常に有名なガリウム砒素，アルミニウム・ガリウム砒素系についても素晴らしい発表を行いました。さらに，非常に多くの種類の材料についても紹介し，シュツットガルトの大学やマックス・プランク研究所が，これらの半導体化合物について分業体制で共同開発している内容についても発表しました。

もちろん，近代の半導体業界とマイクロエレクトロニクスの牽引車であったシリコンについての発表も行われ詳しく論じられました。特に，非常に難しいように見えますが，コンピュータ・サイエンス，コンピュータ・ハードウェア，電気通信に大きなインパクトを与えると思われる新しい開発成果についても紹介されました。

赤坂氏の講演では，半導体分野の人々にとって非常に興味深いシリコン結晶の内部にデバイスを三次元に配置したものが紹介されました。まず，シリコン基板にデバイスの層を乗せ，その上に多結晶性シリコンを重ねます。この多結晶性シリコンを再結晶すると，材料の物理的特性が発揮され，結晶の方向性が非常に重要な役割を果たします。彼は，例えばラマン・スペクトロスコピーを使って，各々の基礎研究がどのような関連性を持っているかの優れた例を紹介しました。このラマン・スペクトロスコピーは，１０年前までは完全に理論的な手法でしたが，今や，非破壊的に迅速に調べられる優れた方法として利用されています。皆様も，赤坂氏と彼のグループが，この三次元デバイスの開発に，大成功をおさめたことがおわかり

になったとおもいます。

もうひとつ，リアルタイムのイメージ変換と光学データ処理に非常にコンパクトで高速かつ内部結合した（inter-connected）デバイスの原理を応用するという発表も注目されました。これも非常に素晴らしい講演であり，材料とそのプロセスを理解することがいかに重要かということを再度認識させられました。この場では，討議の概略だけで，内容にまで詳しく立ち入るつもりはありませんが，各レベルがいかに複雑であるかはご理解いただけたと思います。材料は，この建物のように，全く異なる活動を持ったフロアから作られた非常に複雑な建物のようなものです。ここには，光ダイオードを持つ個々のパーツから始まり，信号処理が進んで三次元に移行します。これは，非常に素晴らしいことです。このように私たちは非常に有意義な話し合いを行いました。また，ミュンヘンのFraunhoufer Societyで始まったプログラムもあったので，意見の交換も活発に行われ，非常に素晴らしい人間的な接触もありました。この研究所で様々なアプローチを試みています。Bauser夫人は，低温での研究を行っています。これは，液晶エピタキシーを作るので，美しく完璧なシリコン結晶が酸化物の上に乗っています。このように個人的な接触，アイデアの交換は非常に素晴らしいものでした。

この他の材料も取り上げられました。ドイツは，化学の分野で優れた伝統がありますが，リソグラフィーとそれに必要な材料についての非常に優れた発表でもこのことが立派に証明されました。発表件数を多くしなかったので，討論の時間が十分取れたと思います。もちろん，発表原稿を選択しなければなりませんでしたが，適切なものを選べたと思います。

最後の発表は，リソグラフ技術としてのイメージの反転(image reversal)で，特殊な光吸収の性質を持たせた誘電分子（die molecule）をこのレジストに使うという，Buhr博士とHoechst-Kalleの同僚研究グループによるものです。ドイツ国内はもちろんのこと，アメリカ，日本などの世界各国と密接に協力しながら行っています。専門家たちも，非常に優れた開発成果であり，写真露出，電子線露出および，X線レジストを使って美しく明解な構造ができることを認めています。このテーマは非常に詳しく論じられ，

複雑なトポグラフィーにきれいな線がかけるという大きな利点があります。これは，ダイナミックＲＡＭだけでなくあらゆる世代のシリコン技術への利用が期待できる高度な集積デバイスの中心課題になることは間違いなく，スリー・ファイブでもこれらの材料を利用しなければならないと思っています。

材料と，その理解，その利用方法について総合的で有意義な議論が行われました。そして，高須氏が，非常に印象深い発表を行いました。これは，一見単純なように見えますが，非常に多くの情報を含んだものです。彼は，次のように述べています。おそらく１０年前には，非常にクリーンなシリコンを作れば，Ｎ－ＭＯＳプロセスでも Ｃ－ＭＯＳプロセスでも，バイポーラ技術でも必要があればどこにでも利用できるだろうと考えられていました。しかし，これは間違っていました。個々のプロセスは，各々，特殊な性質の材料が必要であるということが発見されました。例えば，Ａという業者はプロセスＸだけを対象とし，Ｂという業者はプロセスＹに最も適しているということです。魚には白ワイン，ローストビーフには赤ワインを飲みたいといったようなものです。しかし，ある特定の工場，特定の目的に合わせて設計されたシリコン・ウェーファーを作るということは，基本的材料となるシリコンを非常に明確に理解し，加工技術を考案しなければなりません。テレフンケン社のGraff 博士は，加工中に混入する不純物を除去するために使用している特殊な技術について非常に素晴らしい発表を行いました。デバイスの設計と共に，単に基板材料だけでなく，製造工程全体を通じて，各々に適した材料を考案しなければなりません。技術は，互いに協力しながら発展しますが，各々の部分に個々の科学的アプローチが必要とされます。このことは，非常にはっきりと現実に証明されていると思います。材料やプロセスに対する経験的知識に頼る時代は過ぎ去りました。非常に基本的な原理からこのような問題を理解しなければなりません。扱っているディメンジョンが小さくなればなるほど，これらを深く理解する必要性が高まります。

このことは，従来は研究室でしか必要とされていなかったような基礎物理学に基づく新しいタイプの装置・機器類が生まれ，これが，半導体産業の成功によって不可欠の装置になるということを意味します。

個々の要件に合わせた独自のプロセス技術を考案・制御できるように，材料とプロセス技術の分析は，できるだけ迅速にできなければなりません。この問題について，私たちの討論ではかなりの時間が割かれ，ほとんどの発表で取り上げられました。もう一つの例は松井氏が発表したもので，高エネルギー物理学における非常に高価で魅力的な手段であるシンクロトロン照射です。ご存知のように，ドイツはこの分野に非常に高い能力をもっています。非常に早くからこのことが認識され，また，ドイツには大型加速器や装置の伝統があるため，工学および科学が相乗的に発展しました。ベルリンとハンブルグには，さらに大型の装置とシンクロトロン技術があり，多くの人々がこの研究所にやってきてシンクロトロンについて研究しました。かれらは，帰国して，筑波やその他各地の様々な装置を使って活発な研究を進めています。

ここで，特性を調べるための技術を列記した長いリストを見せます。X線は，非破壊的であるため非常に優れた有用な手段です。サンプルを分解する必要がありません。また，基本的には分光学的方法であるため，非常に多くの情報を包含しています。物質内部で進行している状態を，そのままの状態で観察する透過型X線トポグラフィーについての説明が行われました。材料とプロセス技術を理解するための，平面波を使った平面波トポログラフィーという非破壊的技術も紹介されました。

半導体材料内の様子を知ることは，半導体技術にとって重要な問題です。これは，転移量といって，特定の格子欠陥は非常に重要な意味を持っていると思われます。これは，固体物理学，結晶学，化学の基本的問題であり，転移密度の高いウェーファーと低いウェーファーの写真の対称性を見ればその違いが簡単にわかります。これをもとにしてガリウム砒素の基板を改良して，高速集積回路とオプトエレクトニクス装置に用いるガリウム砒素を作るための膨大な量の研究が日独両国で進められています。

もう一つの例は，小切間氏が発表したものですが，これは，結晶内部で進行している状況を知るための新しい方法です。しかし，これは先にのべた松井氏の写真だと思います。これは，建造中のモノクロメーターですが，新しい装置がどうやって作られるかということを紹介するためにお見せし

ます。これについてはかなり多くの成果が出ており，もっと優れた装置が必要になっています。

小切間氏は，X線の応用例も紹介しました。このようなアルミニウム・ガリウム砒素－アルミニウム砒素のヘテロ接合，カンタム・ウェルを観察する新しい技術を紹介しました。ウェッジを作り，それをX線で観察する〔ＣＡＴ〕と呼ばれる新しい技術を発明しました。これは，化学組成，インタフェースの性質を調べるための非常に高度で感度の高い技術です。このウェッジの写真から，新しいタイプのデバイスの性質を決める材料の性質を調べる手段として利用できる技術の概要が理解いただけると思います。

他の電磁スペクトルの分野にも，迅速，非破壊的に高度な情報を示す分光学的技術があります。これは，本研究所のWeber博士が紹介しました。彼は，私たちの研究所が，よりクリーンで高性能のシリコンを望んでいる人々に新しい方法と手段を提供するために試みている基礎研究の中から，様々な活動を紹介しました。フォトルミネッサンスの強度が，ここに，波長の関数としてプロットされています。これらの線には，非常に多くの情報が含まれています。材料を照射し，そのルミネッサンス強度を見れば，基本的な電子プロセスについて詳細な情報を得ることができます。例えば，シリコン結晶内に作られた炭素対を見ることができます。炭素は，非常に検出が難しく，材料にトーピングすることはありません。また，単なる供与体や受動体ではなく，グラファイトや気体から，材料内に入ると思われます。炭素は，電気的に不活性であるという直接的な理由で重要なのではなく，沈澱の核になるという間接的な理由で重要であり，結晶内の非常に繊細な構造を破壊するおそれがあります。

Weber博士と彼のグループは，この炭素－炭素対から発生する特殊な信号を発見し，この発光信号を使ってシリコン内の炭素検出限界を２桁引き下げることができました。これは非常に重要な成果で，新しいキャリブレーション曲線ができると思います。以前は，１cm^3あたり５～１５原子の炭素濃度しか測定できませんでした。これでも，以前から，あらゆる化学的な方法より非常に感度の高い方法でしたが，G線の強度を使うことによって，感度をずっと上げられることが立証されました。これは，シリコンの

物理学的性質の完全な理解から生まれた非破壊的分光学的方法が非常に有用であることを示す一例です。

シリコン内に含まれる酸素も非常に重要な意味を持ち，研究分野でも開発分野でも非常に活発に研究されているテーマです。酸素の量が，集積回路の成功，不成功の鍵を握っています。世界有数のシリコン・メーカーであるWacker-Heliotronic のWagner 博士が，酸素の作用，例えば，熱供与体（thermal donar）について素晴らしい発表を行いました。シリコン内で特殊な熱が発生すると，酸素原子が集まって結晶内にドーピングします。そして，電気的活性を示し始めます。これらは，熱供与体と呼ばれています。これは，非常に困った現象で，結晶の持っている優れた性質を破壊しますので十分理解しなければなりません。ここに非常に優れた物理学的研究ががあります。エネルギー・レベルを計算した研究ですが，これも私たちの研究所が，産業界と協力して行ったものです。日本人研究者も，非常に高度な技術を使ってこれに参加しています。Wagner 博士は，彼の研究結果についても報告しました。熱供与体のシーケンスである№1と№2の対があると思われます。焼きなましや熱処理を行うと，この対が行ったり来たりします。すなわち，非常に複雑で，複数の原子が関与する分子化学的変化がシリコン内で進行しています。これは，私たちが内部で起こっていることを理解する上で，非常に大きな意味を持っています。もっと小さいディメンションのことを知るためには，これらを見逃すことはできません。個々の物理的性質をよく観察しなければなりません。これは，他の発表でも紹介されました。

ご存知のように，電子顕微鏡は非常に重要な装置です。Siémens の Föll 博士と Oppolzer 博士が，日本製の高分解能電子顕微鏡を使った研究発表を行いました。彼は，電子顕微鏡の様々な応用例について素晴らしい発表を行いました。原子がどの位置にあるのかを知らなければなりません。例えば，この場合のこれは単結晶シリコン上のポリシリコンです。ここに点が見えますが，これは，個々の原子の回折像を表わしています。これが本物の原子と考えることは非常に危険ですから，やめて下さい。これは複雑な回折パターンです。何を見ているかを理解しなければなりません。Föll 博

士は，大型コンピュータを使って根本原理から適切な計算を行って回折パターンをシミュレートしなければ，見ているものが何かを理解することはできないと断言しています。

そして，非常に優れた警告を発すると同時に，実際に見ることができる具体的なフリンジを示しました。これは，専門家を対象としたもので，インタフェースの格子フリンジです。これは非常に重要な意味を持ち，このインタフェースこそが，何か変化が起きる場所です。このインタフェースを理解しなければなりませんし，このような性質は電子顕微鏡の画面の解釈を非常に複雑にしています。ここや，ここで突然フリンジが停止しているのが見えますが，ここでフリンジが終わっているので，ここに転移欠陥があると早急に結論することはできません。これは，彼の発表と分科会での討論の中で学んだことであり，共著者の意見でもあるのですが，ここで，もう一度，科学的なインパクトということを強調したいと思います。すなわち，科学的原理に基づいて完全に理解しない限り，誤解が生じるおそれが大きくなります。

このような測定の中から収集できる情報は非常に重要であると申しあげましたが，研究室から生まれたもうひとつの例を紹介したいと思います。日本の論文のひとつが，マイクロプローブ反射の素晴らしい例を紹介しています。すなわち，高エネルギー電子を使い，これを反射させれば，材料内の状況を知ることが出来るというものです。ここで，小切間氏は，全般的にますます小さなディメンションに進んでいく傾向があると述べています。この場合は，データを高速で取得する（acquisition）能力をもつ非破壊的な手段だけでなく，電子顕微鏡と同じように，できるだけ小さいディメンションに進んで行かなければなりません。私たちは，結晶が成長する時の個々の非常に小さい結晶点を非常に丁寧に観察するマイクロプローブ反射の研究結果に大きな感銘を受けました。

何度も何度も繰り返されたテーマは，材料と材料のエピタキシーを理解し，製造することが非常に重要なポイントであり，この材料の特性を決定するということです。この二つは切り離すことはできず，私たちの議論では，これについての素晴らしいアイデアが交換されました。そして，お互

いに強い影響力を及ぼしました。田中昭二教授と彼の研究グループの発表は，非常に優れたものでした。ドイツ側参加者になり代わり，日本側の出席者全員に感謝したいと思います。非常に熱心な討議が繰り広げられました。ご参会の方々に感謝したいと思います。意見の交換は非常に実りあるものでした。

4. 閉　会　挨　拶

4. 閉 会 挨 拶

4.1 新 欣 樹 通商産業省機械情報産業局電子政策課長

〔閉会挨拶〕

エングル先生，柳井先生，トーマスさん，そして，ご列席の皆様！ まずはこのフォーラムに参加された皆様が２日余りにわたるハードスケジュールを成功裏に終えられたことに対しまして敬意を表したいと思います。

ただいまの３つの分科会のサマリーレポートを伺いまして，今回のフォーラムがたいへん有意義であったとの感を深くしたしだいでございます。とくに，従来の情報技術分野における研究成果の情報交換に加えまして，今後の日独両国間の研究交流や共同研究の可能性といったことにつきましても検討をいたしましたことは，今後のこのフォーラムの役割を方向づけますうえできわめて重要な契機になったと認識をいたしたしだいであります。

このように，今回，多大な成果を得ることができましたのも，エングル，柳井両議長，親愛なるトーマス氏をはじめＢＭＦＴの皆さん，および日独双方の主催者の皆様の周到なる準備とご努力の賜物であると考えます。

次回のフォーラムは来年の１１月に京都か奈良で開催されるとのことでございますが，その際には今回同様，有意義かつ活発な交流がなされることを期待するしだいでございます。ダンケシェーン。

4.2 U. トーマス 研究技術省第４局次長

〔閉会挨拶〕

このフォーラムを終えるに当り，一言ご挨拶を申し上げたいと存じます。

この活動が年々盛んになってきて嬉しく存じます。私共は，ますます得るところが増えてきているという印象を持っています。議論百出致しましたが，明らかにレベルの高いものでした。お互いに議論ができ，しかも非常にオープンに議論できるという信頼感が増してきております。この事はいつも重要な事でした。

また，うれしい事に，ドイツ側のＧＭＤと日本側のＪＩＰＤＥＣの間の協力で，今回のフォーラムの準備から実際の運営まで，順調に行われたと思

います。この場をかりまして，GMDとJIPDECの皆様のご尽力に対し感謝の意を申し上げたいと存じます。といいますのも，その仕事は決して簡単なものではなかったからです。このように困難で複雑な事柄を組織化し，運営する場合には，いつでも距離というものが重要な要素となります。今回のフォーラムの準備から運営まで参加して重要な役割を担ったわれわれドイツ側の1人は，近い将来，東京に赴任することになっております。その結果，両国にとって非常に良い，情報技術のための橋渡し役となるでしょう。

率直に申し上げて，この会場には研究関係の官庁の方が何人かいらっしゃっていますが，私共にとってこの種の行事は大いに役立つものだと申し上げたいと思います。と申しますのは，これによって，情報技術の分野での研究を促進するに当っては，関係官庁からの視点も含めて，一体どういった種類の取り扱い方が，適切なものなのかという事について思いめぐらしているからなのです。私はまた，新電子政策課長より，どのように日本の通商産業省がきめこまかく自国の産業を指導しているかを教えてもらおうとも致しましたが，いくつかの詳しい説明をいただきましたので，われわれの参考にさせていただきたいと思います。

次回のフォーラムは日本でというご招待にはうれしく存じます。私共皆よろこんで参加したいと思いますし，なによりも当然のことながら，このフォーラムの使命の一つは，科学者・技術者の交流，科学技術の交流にあるのだと申し上げたいと思います。また，両国の友情を深めるという使命もございます。このことは，この席を貸りまして，率直に申し上げたいと思います。私共は，ドイツと日本の科学者同士の友情を深めたいと思っていますが，それは先ず，第一に科学者自身のためになるからであり，かつ私共両国のためにもなるからだと思っています。さらに申し上げれば，次回のフォーラムは，今回よりも一層中味の濃いものとなり，われわれが若い科学者の人達に日本で仕事をしたり，反対に日本の若い科学者達に，このドイツ連邦共和国で仕事ができるような，もっとたくさんの可能性を与えるにはどのようにしたら良いのかという事について，議論をすることになるでしょう。これは必ずしもやさしい事ではないのはもちろんですが，言葉の

壁，まあわれわれドイツ側からの方が，ひょっとしたら日本の科学者よりも躍び越えるのが難しいかも知れませんが，このような壁があります。しかし，もちろん，相互に知り合う事が重要であり，そこではおたがいに最善の形で出会うことができると思います。そして思いますに，このフォーラムの場で両国の科学者にもっと相互の交流のチャンスを与え，日本とドイツで共同研究作業をしてもよいという時期が今，熟してきたと思います。そして，この基礎をここにうち建てるお役にたてたことと思います。このことは誰しもが願っていることです。

また，お礼申し上げなければならないのは，民間企業からこのフォーラムに参加して下さった方々です。この場を借りまして厚くお礼を申し上げたいと思います。多くの民間企業の方々の参加がなければ，今回のフォーラムの価値は間違いなく半減したことでありましょう。

新電子政策課長，さて最後にもう一度言わせていただきたいと思いますが，私自身非常にうれしく思うのは，日本の通商産業省とのコンタクトが年々密になって，また他の通商産業省の方々とも面識を得る機会ができたということなのです。私自身の側からただ申し上げたいのは，…というのは皆様に申し上げたいのですが，エンゲル先生がまだこれから閉会の辞を述べられますので，…皆様方，帰路つつがないよう，そしてまたここにお越しいただいたことを再度お礼を申し上げたいと思います。この当地にて，お骨折りいただいたのは，クワイサー教授と研究所の皆様ですが，ボンから参りました私共に対して温かくおもてなしいただいたことについてお礼を申し上げたいと思います。われわれは，本当にバーデンビュルテンベルク州とこの研究所をおとずれてよかったと思います。われわれは皆来年日本でお会いできることを本当に楽しみにしております。ご清聴ありがとうございました。

4.3 W. L. エングル　　ドイツ側議長　アーヘン工科大学教授

〔閉会挨拶〕

皆様，お疲れさまでした。せっかくおいでいただきましたのに，十分な

お世話もできませんで失礼いたしました。次のフォーラムではまたお互いに頑張りましょう。無事お帰りください。ありがとうございました。

5. ニューメディア分科会アブストラクト

5. ニューメディア分科会アブストラクト

LOW- AND HIGH-VOLTAGE THIN FILM TRANSISTORS FOR ADDRESSING FLAT PANEL DISPLAYS

Prof.Dr.-Ing. Ernst Lüder

Each picture element (pel) of a liquid-crystal-flat-panel display (LC-display) is, as a rule, addressed by a circuit consisting of a thin-film transistor (TFT) and a storage capacitor. Fabrication processes and performance of CdSe-TFT's and a-Si-TFT's are reported. Both transistors possess a double-layer gate-dielectric out of anodized Ta_2O_5 and evaporated or CVD-SiO_2. Due to a three-step annealing process the CdSe-TFT exhibits very good properties, namely a mobility of 160 cm^2/Vs, a switching ratio $R_{off}/R_{on} = 10^9$, and an $I_{off} = 0.1$ pA at 3000 lux. A 12 000 pel-display was fabricated with and, for the first time for CdSe-TFT's, also without storage capacitors. The latter was feasible because of the low I_{off}. The display without storage capacitor provides a higher contrast and a wider viewing angle than the display with C's. This is achieved by the elimination of a parasitic capacitive voltage divider. Optimum contrast without storage capacitors is 1:48, the viewing angle for a contrast 1:16 resp. 1:8 is 45° resp. 50° in horizontal direction. Pel-yield was 99.8 % inspite of fabrication in a non-dustfree laboratory. This stems from a robust fabrication process and from overdesigning the devices. The self-healing property of anodization virtually eliminates failures in the dielectrics, whereas the TFT's could be built to withstand 100 V and to switch in 1 μs, both exceeding the requirements for LC-displays.

The high voltage CdSe-TFT is based on reactively sputtered Ta_2O_5-dielectric which is anodized afterwards in order to withstand 400 V. The spread in break-through voltage was very narrow with a standard deviation of $\sigma = 0.05$. This TFT was used to address a PLZT-light valve with a switching time ≤ 1 μs. The high voltage TFT is also suitable for addressing VF- and EL-displays, where the high currents of CdSe-TFT's of 500 μA per 100 μm channel-width are actually required. The current in a-Si-TFT's with SiO_2 or SiN as gate dielectric amounts to about 3 μA per 100 μm channel-width. In a-Si-TFT's with Ta_2O_5-dielectric the current was enlarged to 12 μA per 100 μm due to the higher dielectric constant of Ta_2O_5, even though a double layer dielectric of Ta_2O_5 and SiN was used. In all cases the TFT's had the same thickness of the gate dielectric. A comparison between the CdSe-TFT's and a-Si-TFT's will conclude the talk.

A Large Full-Color Flat Panel Display for HDTV

Teruo Hirashima

NHK Science and Technical Research Laboratories, Tokyo, Japan

1. Introduction

HDTV is an entirely new television system which fullfills viewer's demand for a high quality, wide screen picture. It transmits five times the amount of information received by conventional television. It has a sense of presence and reality, and has a great impact on viewers.

26~40-inch CRTs and 50 ~400-inch projection type displays were already developed for HDTV, but for home-use a thin flat panel display is preferable because of space and weight.A flat panel is an ideal display, but there are many problems not yet solved and its research and development still has a few risks.

The development of a flat panel for TV is more difficult than for data-graphics, because TV display requires full-color, good grey tone and high speed of response.

2. Current technologies

Table 1 shows an example of specifications required for HDTV display and Table 2 the comparison of devices used for a flat panel for HDTV on the specifications shown in Table 1.

(1) Plasma display panel (PDP)

PDP is most promising for a meter-size, large panel.Its feasibility depends upon the precise fabrication technology. Because of limited resolution due to areas occupied by phosphor and cell barrier, full-color PDP is not suitable for a small panel.It is superior to CRT when its size is over 40-inch-diagonal large panel. To produce tri-color, PDP uses UV rays to excite phosphors,but luminance and efficiency are not sufficient because of a small pixel volume. It is necessary to search for gas composition and discharge mode to radiate more intense

UV rays with higher efficiency.

(2) Electroluminescent display (EL) and light emitting diode (LED)

The main bottleneck of EL and LED for a full-color panel is a poor blue light emission, and the basic research has to be done to find out new materials.

ZnS:Mn and SrS:Ce were reported as blue light emissive EL materials, but ZnS:Mn has insufficient luminance of only 3 ft-L and efficiency of 0.002 lm/W and SrS: Ce is not good in blue color purity.

In the case of LED, SiC, GaN, ZnSe and ZnS which have a bandgap over 2.6 eV were developed, but none of them have obtained sufficient luminance as yet.

(3) Flat CRT and vacuum fluorescent display (VFD)

High(5~30 kV) or low(50~150V) voltage cathodoluminescence is utilized to obtain high brightness and good color.In conventional CRT, an electron gun has to be placed far from the screen, to obtain a wide deflection angle of electron beam. This makes CRT bulky.

Various concepts of a flat full-color CRT have been investigated, but none of them are successful.

In the first type of flat CRT developed by U.K. Philips, electron beam scanning and energizing function are separate. Its scanning system is housed in a flat package, because a low energy electron beam is easily deflectable, and a large area channel multiplier is used to get high energy electrons which excite the phosphor screen. In this way, monochrome panel of 12 inch screen 75 mm deep was developed.

The second approach of flat CRT was made by Matsushita. It uses multi-line filaments instead of a single gun and several kinds of line electrodes for adressing and modulation. A full-color panel of 10-inch screen 65 mm deep was developed. This structure is similar to VFD.

The third concept of flat CRT utilizes two dimensional gas discharge cathode or plasma cathode, as an electron source, which was reported by Siemsns (11.5-inch screen 60 mm deep) and Lucitron(35-inch screen 5 inch deep).

In all three cases, spacers must be used to be pressure resistant so a new

concept should be introdused for the sake of compatibility of high resolution and a large area screen. Furthermore it is very difficult to fabricate complicated electrodes throughout a meter-size panel. From these viewpoints, a plasma cathode flat CRT is most promising for a large flat panel. VFD has a problem in power consumption when it is made large.

(4) Liquid crystal display (LCD)

LCD has attractive features: flatness, low power consumption, low voltage drive and good full-color. But in the twisted nematic(TN) LCD which is now widely used for many purposes, the contrast greatly decreases as scanning line increases owing to an inevitable crosstalk between pixels on the same line. To avoid this, active adressing was investigated to separate each pixel by an electrical switch. A thin film transistor (TFT) is currently used as a switch.

At present 2~4 inch active adressed portable TV receivers are commercialy available. Its size will increase 14 inches in five years, but defect and uniformity will be more significant.

3. A 20-inch full-color PDP developed by NHK Laboratories

Recently NHK Laboratories developed a 20-inch panel of which size is the biggest as a full-color PDP. It is a pulse discharge memory panel of simple structure which is favorable for a large panel (Fig.1). Its luminance is rather low (about 30 cd/m) but it is most feasible to achieve a large panel.

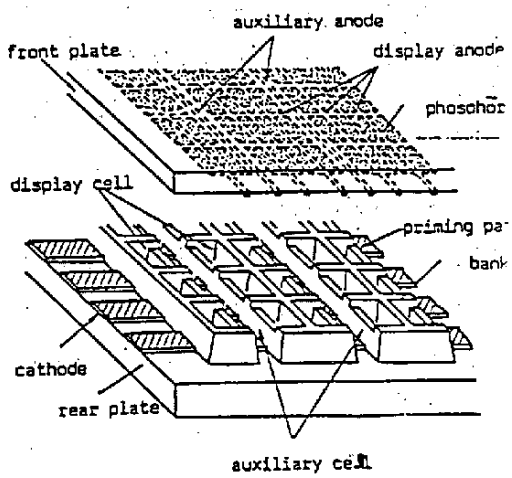

Fig.1 PDP of a simple structure

Table 1 Disirable specications of HDTV display

Scanning line	1125
Field frequency	60 Hz
Aspect ratio	16 : 9
Screen size	0.8 m (vertical) x 1.4 m (holizontal)
Viewing distsnce	2.4 m (three times screen height)
Horizontal viewing angle	30°
Luminance	150 cd/ m^2
Contrast ratio	70 : 1
Luminous efficacy	1.5 lm/W

Table 2 Characteristics of devices for a HDTV flat panel display

	screen size	definition	luminance	full-color	thickness	power consump.	total
P D P	◎	○	△	◎	◎	△	○
E L	△	○	△	×	◎	△	×
L E D	△	△	○	×	○	△	×
Flat C R T	△	○	◎	◎	△	○	△
V F D	×	△	○	○	△	△	×
L C D	△	○	○	○	◎	△	△

◎ excellent, ○ fair, △ good, × not good

Materials for colour TV based on Liquid Crystal Technology

Dr. U.-H. Felcht

The fast development of high information Liquid Crystal Displays involves new challenges for chemical material science. The complex construction of a Liquid Crystal Display requires specially optimized materials. They must be compatible both as regard to the production of the displays and in its functions. In this case it is desirable that the chemical industry develop a balanced product package for the electronic industry. Of particular importance for high information color LCD's (TV) are new fast switching liquid crystals, optimized orientation layers, photoresist-materials, high density color-pixel filters and sealing materials.

Ferroelectic, smectic C*, liquid crystals are basically characterized by fast switching time, bistability and improved contrast ratio. Unsolved problems concerning bistability, grey scaling and shockproof are being worked on very intensively. Solving the problems from the chemical angle offers many advantages against the TFT/nematic-technology. The high density colour-pixel filters can be produced by structurized dye printing techniques or by electrophoretic methods. Photoresists and Sealings have to be compatible with LCD materials during processing steps.

F L A T C R T

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Introduction

A considerable amount of effort has been made to develop a variety of flat CRTs in the past decade. The progress made in the field of color technology has been remarkable. Nevertheless, we still do not have flat color CRTs, which are up to the standards of quality set by conventional CRTs, put into practical use. In this paper, present status and some considerations on future of flat CRTs are described.

Types of flat CRTs

Various types of flat CRTs have been devised since Aiken Tube and Gabor Tube back in the nineteen-fifties. The types of flat CRTs may be classified into three groups according to the structure of cathodes as shown in Table 1. Five typical types from Table 1 are shown in Figs. 1-5.[1)-5)] One of these types, namely, Matrix Drive and Deflection System (MDS) flat CRT reported by the author in 1985 will be described in some detail referring to Fig. 1. In the MDS flat CRT, 3000 controlled beams are formed by means of a matrix of 15 horizontal filament cathodes and 200 perpendicular electron beam control electrodes. Each beam is horizontally deflected in 6 steps (two sets of R.G.B.) and vertically deflected in 32 steps (including the interlace) to form an image consisting of 192,000 elements on the display panel. A complete picture is formed by means of a line-at-a-time method.

The inherent advantages of MDS flat CRT are :

1) Flatness of the screen and good linearity of the picture,

2) Good uniformity of the beam focus throughout the screen,

3) Freedom from convergence problems,

4) High resolution and high brightness,

5) Possibility of a large screen panel with a self-supporting structure.

Some considerations on future of flat CRTs

The important factors in realizing a color flat T.V. are :

1) Uniformity of beam current,

2) Uniformity of beam spot size and shape,

3) Accuracy of beam landing position.

Lack of any of these factors results in poor image quality.

In a single-point cathode type, he beam current is uniform in principle. In multi-cathodes or area cathode types, it is necessary to take some measures for realizing above mentioned three requirements. It may be a feedback system for beam currents, or application of dynamic focusing voltage, or the beam index'system, for instance.

No matter what the size of the conventional CRTs is, the basic principle is the same shadow mask system. While there can be a number of different types in the principle of flat CRTs.

The future principle of flat CRTs will be not necessarily one but a number of types according to the screen size, resolution, etc., of the display. In any case, certain measures would be incorporated to realize the above mentioned three requirements.

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Table I Classification of flat CRTs

Cathode type	Types of flat CRT	Companies who investigated
Single-point cathode	(1) Flat CRT with a side gun (2) Channel Multiplier Flat CRT	Sony, Sinclair, Hitachi, Sanyo Philips
Multi-cathodes in line	(1) Guided-Beam Flat CRT (2) H-addressing and V-deflection system	RCA Kanazawa Inst. of Tech.
Two-dimensional area cathode	(1) XY matrix addressing (i) VFD (ii) Hybrid Plasma Flat CRT (iii) Microtips FD (2) Matrix Drive and Deflection System	Ise, Futaba, NEC, Hangzhou univ. Lucitron, Siemens LETI-IRDI-Commissariat a I'Energie Atomique Matsushita

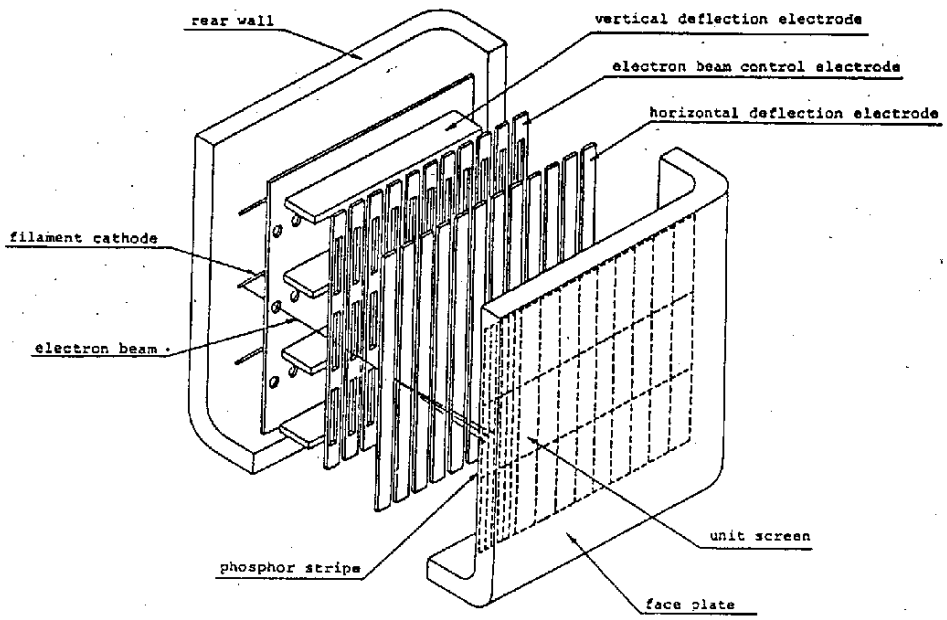

Fig.1 MDS flat CRT
(Matsushita)

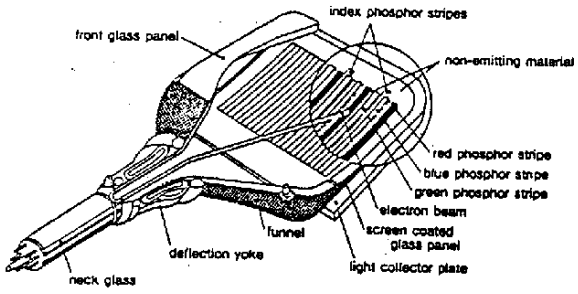

Fig.2 Flat CRT with a side gun

(Sanyo)

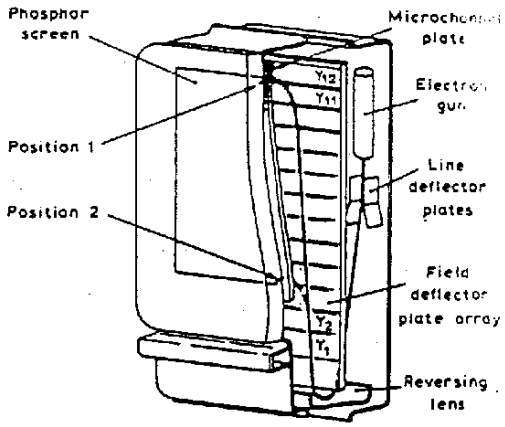

Fig.3 Channel Multiplier Flat CRT

(Philips)

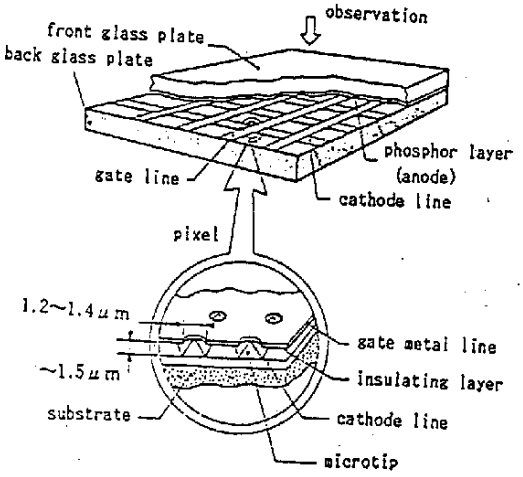

FIG.4 Microtips F. D.

(Leti-IRDI-CEA)

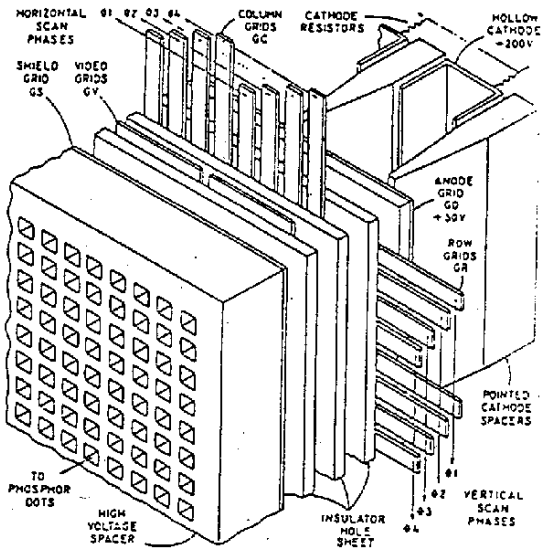

Fig.5 Hybrid Plasma Flat CRT

(Lucitron)

SOLID-STATE LIGHT VALVES

R. Gerhard-Multhaupt

Light-valve projection represents a proven technique for the display of large and bright high-resolution video images. The centerpiece of a light valve is a spatial light modulator which modifies the light from a suitable source by means of reflection, refraction, birefringence, diffraction, or scattering. Addressing and control of the spatial light modulator is achieved with electron beams, light beams, primary images, passive or active matrices. The resulting light modification consists of spatially varying changes in the propagation direction, the phase, or the polarization and is transformed into the required intensity modulation by input and output filters that also absorb the light not required for the desired image.

In this talk, several spatial light modulators and addressing techniques, as well as combinations thereof, are discussed on the basis of commercially available or experimental light valves. Solid-state technologies are emphasized, since they promise compactness, fast response, reliability, high resolution, and full integration of light-control and addressing devices.

Control layers modulating the phase or the propagation direction of the incoming light are used in a Schlieren optical system which provides for the required intensity modulation of the output light. Examples of such devices include deformable layers of fluid or viscoelastic materials, liquid-crystal cells or electro-optic substrates which scatter or diffract light, and deformable mirrors or membranes.

Spatial light modulators, which are based on electrically induced birefringence, change the polarization state of the light and thus necessitate polarization optics for the desired conversion to intensity-modulated light. This control-layer category encompasses twisted-nematic (TN), highly (HBE) or super-twisted birefringence-effect (SBE), and surface-stabilized ferroelectric (SSFLC) liquid-crystal cells as well as electro-optic layers from anorganic or organic crystals, ceramics, and guest-host polymers.

Addressing and control of the spatial light modulators may be effected by electric field variations, which are in turn generated by electron-beam-deposited charge distributions, light-beam- or image-induced photoconductivity patterns, externally driven row and column electrodes, and matrices with active elements for each pixel.

Our goal, the active-matrix-addressed solid-state high-resolution spatial light modulator, represents the counterpart to the solid-state imaging device already available. It may be used not only for the light-valve projection of large images, but also e.g. as an input or filtering device in optical-signal or image processing applications, as coherent-to-incoherent, incoherent-to-coherent, or wavelength converter, as a light-controlling element in adaptive optics, and as a routing and switching device for optical interconnections.

High-definition Television Transmission in Telecommunications

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Since HDTV's bandwidth is very wide compared to that of existing TV system, wideband transmission including bandwidth reduction coding is essential.

Signal formats and coding schemes for HDTV are shown in Fig.1. The history of HDTV video technology development in Japan is shown in Fig.2. We have already developed 20 MHz Time Compression Multiplexing (TCM) video signal. The two bandwidth reduction technologies being developed in Japan are "MUSE" and "High-efficiency TCM (HE-TCM)". In the future, burst coding, whose bit-rate is variable, would be one of the most important technology in Asynchronous Time Division (ATD) network. HE-TCM signal as shown in Fig.3 is obtained by adaptive sub-Nyquist sampling (subsampling) with intrafield and interframe interpolations. This method reduces HDTV signals to 8 MHz bandwidth, and these compressed signals are converted to 90 ~ 130 Mb/s digital HDTV signals by also applying DPCM or PCM coding technologies.

In telecommunications, there are various types of large-capacity transmission systems applicable to HDTV transmission: optical fiber cable, coaxial cable, satellite, and terrestrial radio transmission systems. Optical fiber cable transmission and satellite communications technologies, which are especially attractive for HDTV transmission, have already been developed. Table 1 shows the NTT's optical fiber cable transmission system (land system). The F-1.6G system, which has the transmission capacity of 1.6 Gb/s, has already been developed as a large-capacity transmission system. Furthermore, coherent optical transmission technologies are now under study. Figure 4 shows recent trends in long-distance, super large-capacity optical transmission experiments. By using new super large-capacity transmission, HDTV signal can be transmitted more economically. Analog high-efficiency TCM signal and digital adaptive predictive coding technologies are under development for application to HDTV. As digital equipments such as HDTV receivers become smaller and their power consumption is reduced by VLSI technology, HDTV transmission service becomes more and more economical.

Figure 5 shows the HDTV transmission concept for the future. HDTV broadcasting signal will be distributed to customers using a direct broadcasting satellite system, communications satellite and optical fiber cable transmission systems. In addition, since HDTV signal will be transmitted nation-wide, various applications of the HDTV system will become available.

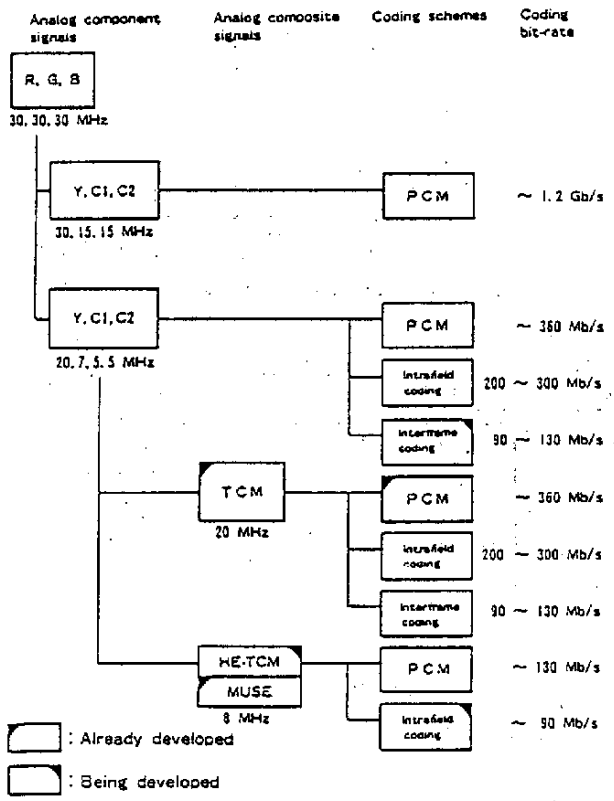


Figure 1 Signal formats and coding schemes for HDTV system

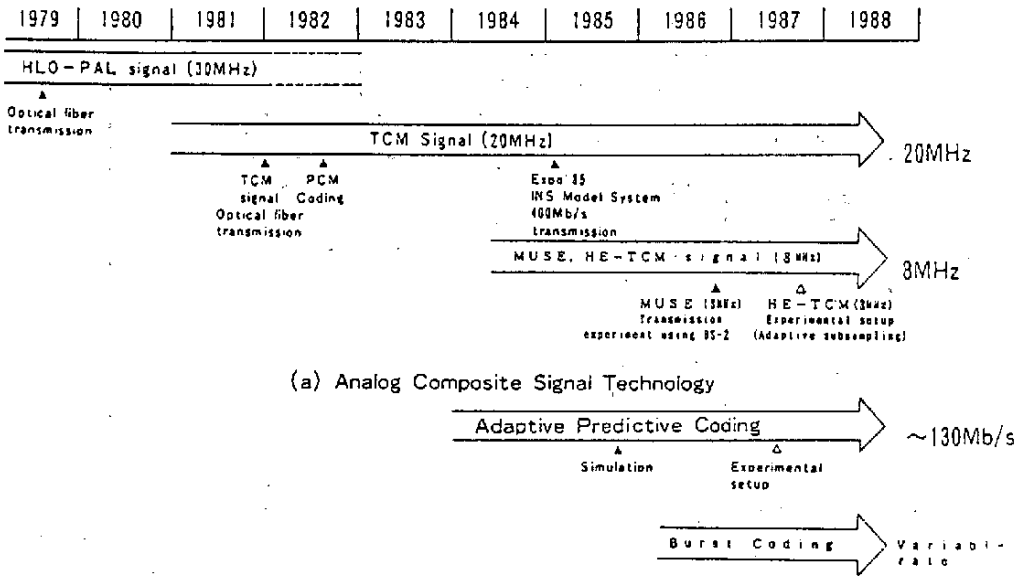


Figure 2 Development of HDTV video technologies

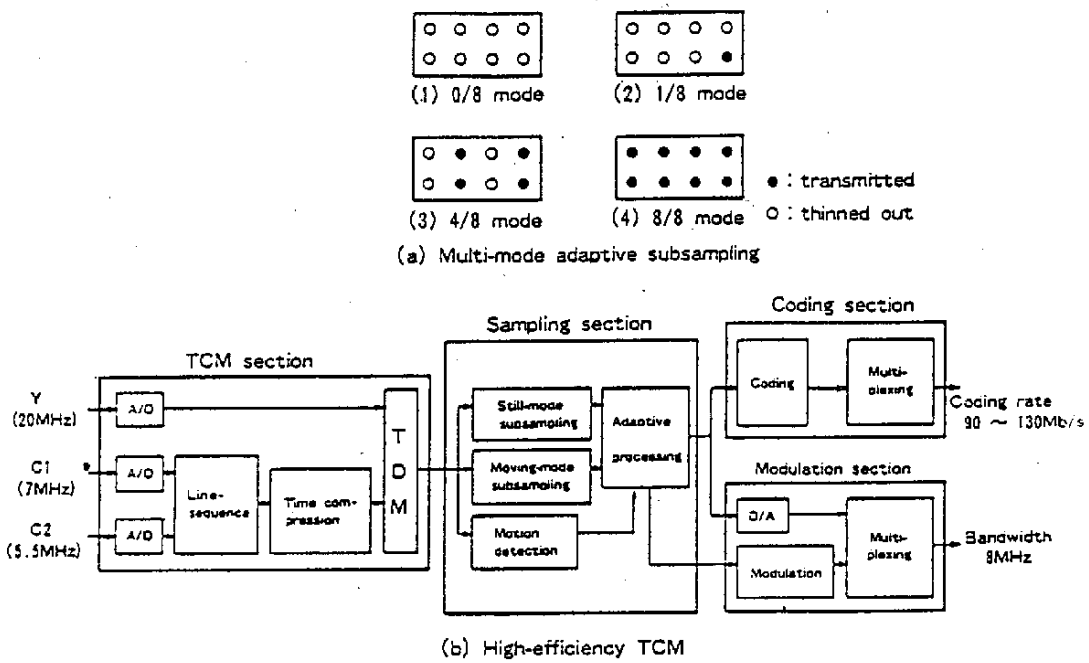


Figure 3 High-efficiency TCM

Table 1 Optical Fiber Cable Transmission System (Land system)

	F-6M	F-32M	F-100M	F-400M	F-1.6G
Line Code	CMI		8B1C	10B1C	
Information Bit-rate	6.312Mb/s	32.06Mb/s	97.728Mb/s	397.200Mb/s	1.5888Gb/s
Line Bit-rate	12.624Mb/s	64.128Mb/s	111.689Mb/s	445.337Mb/s	1.7833Gb/s
Capacity (64Kb/s Tel.)	96ch	480ch	1440ch	5760ch	23040ch
Wavelength	1.2, 1.3 μm	1.3 μm			
Optical Fiber	GI		SM		
Source	InGaAsP LD				
Detector	Ge-APD				InGaAs-APD
Repeater Spacing	15 km	10, 15, 25km	25, 30 km		
Bit Error Rate /Rep.	10^{-10}	10^{-11}			

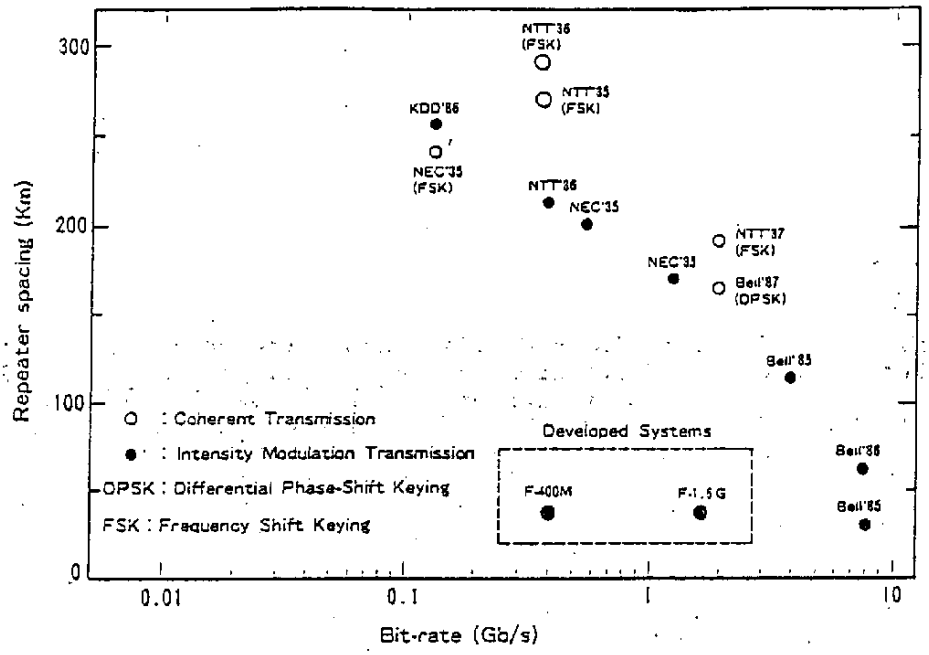
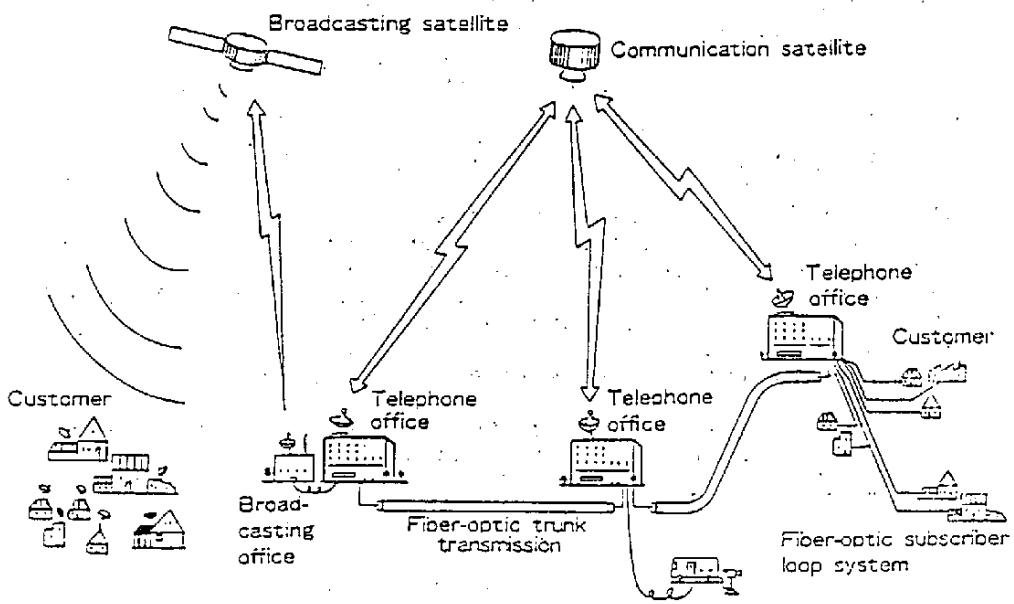


Figure 4 Recent trends in long-distance large-capacity optical transmission experiments



Figaure 5 HDTV transmission concept for the future.

Review of Proposals for HDTV Transmission

Dr. Ludwig Stenger

Abstract

The contribution is subdivided into three sections. In the first there is a discussion of the transmission media available or under active research. Usefull satellite bands at 12 GHz, 22 GHz and 42 GHz are considered and the characteristics of channels allocated during WARC '77 and the status of the planning efforts in the European Broadcasting Union (EBU) for 22 GHz are explained. Alternative approaches by medium power satellites are indicated. HDTV transmission in the "hyperband" of CATV systems and in future broadband ISDN systems based on optical fibre technology are discussed. TDM system proposals and the status of work on coherent optical transmission systems are considered.

In the second section transmission formats for 12 GHz-WARC-type channels ("smallband channels") and for channels above 12 GHz with a "wider" RF bandwidth are discussed. Signal processing techniques, necessary to adapt the original HDTV signal bandwidth to the available channels are considered too. Rather sophisticated motion adaptive filtering and subsampling techniques have to be used for the transmission of HDTV through WARC channels by MUSE and HD-MAC (Eureka, EU 95). There are less stringent signal-processing requirements in case of two-channel systems, of wideband MAC-compatible techniques and of wideband non-compatible, revolutionary systems. Digital assisted televison (DATV) is a usefull technique in all applications.

All-digital solutions are possible in 22 GHz satellite channels and on the optical-fibre based B-ISDN. For that, source coding techniques for data-rate reduction have to be investigated and appropriate modulation and multiplexing schemes have to be considered. In Europe these subjects are dealt with in supra-national projects RACE and COST 206. Some of the proposals made there are outlined.

In the third section the status of research and implementation work is reviewed and a scenario for the introduction of a HDTV service is outlined.

PROGRESS IN HDTV RECORDING TECHNOLOGIES

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The HDTV analog VTR has been available for practical applications for a period of 4 years. However, the picture quality is not yet fully satisfactory because of limited bandwidth, relatively low signal to noise ratio, and picture quality degradation due to multiple generation dubbing. In order to cope with these difficulties, the advent of the HDTV digital VTR is strongly desired. This paper describes the recent technical progress in our HDTV digital VTR development.

In 1985, we developed an experimental HDTV digital VTR with a bit rate of 1.037 Gbps in an effort to realize a high quality production-use VTR. This machine successfully demonstrated the feasibility of such ultra-high speed recording. However, the signal parameter values were chosen principally for experimental purposes. The results from this experimental VTR were presented at the 3rd Germany Japan Forum on Information Technology in Tokyo, October 1986.

In May 1986, the CCIR reported the proposal for a new recommendation of parameter values for HDTV in Report 801. Although no accepted, these parameter values are the only ones available so far, and it is necessary to confirm the technical feasibility of digital tape recording through the extensive study of high speed recording technology.

With some modifications to our previous machine, we succeeded in realizing an experimental HDTV digital VTR with a total bit rate of 1.188 Gbps. By adopting a luminance sampling frequency of 74.25 MHz, that is 5.5 times the 13.5 MHz sampling frequency of CCIR Rec. 601. the proposed parameter values in the CCIR Report 801 have been fully satisfied. Using the same number of 8 recording heads as the previous machine, the recording rate per channel is 148.5 Mbps and the minimum recording wave length is 0.69 μm. The measured S/N at the decision point is approximately 26 dB(pp/rms) and the raw bit error rate is roughly 2.5×10^{-5}. Using the error control mechanism based on Reed-Solomon product code with overhead for parity, sync code and ID code included in the blanking period, the errors are almost completely corrected to the level sufficient for practical applications. Even after 20th generation dubbing, no picture quality degradation has been observed.

Further distinctive features of this newly developed machine are: 8 channels of professional quality digital audio sampled at 48 KHz with 16 bit/sample linear quantization recorded on 8 longitudinal tracks, and reduced processor size by utilizing VLSI chips developed for the 4:2:2 digital VTR and other advanced semiconductor devices.

Table 1 shows the parameters of the new experimental HDTV digital VTR.

In conclusion, the development of a new experimental HDTV digital VTR which meets the draft HDTV studio standard shown in CCIR Report 801 has verified that ultra-high speed recording and playback at 1.188 Gbps is feasible.

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Table 1. Parameters of the experimental HDTV DIGITAL VTR developed in 1987

Mechanical and Tape Format	
Tape	Metal particle type (Hc:1440 Oe, Br:2150 G)
Tape width	1 inch
Tape speed	805 mm/sec
Recording time	1.0 hours using 11,75 inch reel with 18 μm thick tape
Video Recording	
Head	Recording: Sendust sputtered type Playback : Ferrite
Head gap length	Recording: 0.35 ~ 0.4 μm Playback : 0.25 ~ 0.3 μm
Track pitch	37 μm
Track width	Recording: 34 μm Playback : 27 μm
Number of channels	8
Drum speed	7200 rpm
Audio Recording	
Head	Recording: Thin film type Playback : Ferrite
Hed gap length	Recording: 1 μm Playback : 0.65 μm
Track pitch	400 μm
Track width	Recording: 360 μm Playback : 200 μm
Number of channels	8 (max) one channel per one track
Video Signal Format	
Video bandwidth	Y 30 MHz R-Y 15 MHz, B-Y 15 MHz (recorded simultaneously)
sampling frequency	Y 74.25 MHz R-Y 37.125 MHz, B-Y 37.125 MHz
Quantization	8 bit/sample, linear
S/N	58.8 dB
Data rate	1.188 Gbps
Error Control	Error correction using a Reed-Solomon product code: Error concealment using an adoptive method
Channel coding	Scrambled NRZ;8-8 conversion
Minimum recording wave length	0.69 μm
Audio Signal Format	
Sampling frequency	48 KHz
Quantization	16 bit/sample, linear
Error control	Cross-interleaving with CRCC
Channel coding	HDM-1

M. Hausdörfer

Pickup Tube or Solid State Imager
- Alternatives for HDTV Image Signal Generation? -

At first glance, this subject does not seem to be of immediate interest - because the pickup tube with semiconductor target stands on the summit of its technology and the silicon solid state imager, used in colour television cameras, steadily gains attention and its share of application. The outcome of this match is predictable.

All this is true for standard television.
High resolution picture taking systems with signal bandwidths of more than 20 MHz - as the HDTV systems use - are continously fighting aperture losses and the impairment of signal to noise ratio, besides other aggravations due to registration problems, etc.. In addition, there is the basic demand for an unchanged sensitivity of the HDTV camera as compared to the standard TV camera.

The silicon solid state image sensor is provided with some features in signal generation, which the pick up tube does not possess. But both devices considerably differ in the characteristics of the noise spectrum that influence the subjective weighting of the perceived noise of the displayed picture.

This contribution deals with the relations of picture signal generation and signal to noise ratio taking the limited definition capability of the pick up device into consideration.

Mr. Hori

GENERAL INFORMATION ON THE HDTV SYSTEM

The high definition TV (HDTV) system has been rapidly introduced into broadcasting and other industrial uses.

The HDTV system is being tested in experimental broadcast via the BS-2 satellite in Japan, and is expected to come into use in covering the 1988 Olympic Games.

From the viewpoint of practical use, state-of-the-art technology has not necessarily been embodied in the hardware for the HDTV system. It seems that only part of potential basic technology has been put to practical use. The realm of technology for the most part sill remains to be explored.

The following is the latest information on the camera which plays one of the important roles in the HDTV system.

[Sensitivity and S/N]

The typical sensitivity of current HDTV cameras on the market is equivalent to F3.2 at an illumination level of 2000 lux. The low sensitivity was one of the most important problems since it was lower by 1 to 1.5 stops than that of the broadcasting cameras currently in use. Among factors that have helped solve this problem are the development of a new pickup tube and improvement in transmittance of beam splitting prism and the performance of the pre-amplifier connected to the pickup tube. As a result, the sensitivity has tripled to F5.6 at 2000 lux, and the S/N ratio of 44 dB has increased by 5 dB to 49 dB. Naturally, the improvement in S/N ratio can translate into an increase in sensitivity.

[Resolution and Lag]

At present, the resolution of a still picture can be said to be acceptable.

The problem is dynamic resolution deterioration. It is related to the pickup tube lag. In this respect, a remarkable improvement has been attained; the new pickup tube has attained resolution comparable to that of the current broadcasting cameras.

[Digital DTL]

A digital DTL is not necessarily essential for the current broadcasting system so that an analog DTL serves the purpose. However, the digital DTL is indispensable to the HDTV system that involves great difficulty in generating the DTL signal and needs elaborate operations. It should be noted that the hitherto prohibitively expensive DTL now cost half as much as before due to advances in semiconductor technology and use of less expensive devices.

[Size Reduction of Camera]

Generally, the TV camera can be reduced in size through simplification of the circuitry, employment of ICs, and reduction in power consumption.
The greatest of all advantages of a compact camera is a reduction in price.
However, it seems almost impossible to develop the camera that at once meets the performance requirements of the HDTV system and equals the so-called "handy cameras" which are in wide acceptance in the current TV system.
How much can the camera be reduced in size at the present technical level?

[Lens]

The image reproduction by the HDTV system is fraught with many problems (e.g. longitudinal chromatic aberration, lateral chromatic aberration, and distortion). The details will be given later. Briefly, any zoom lens currently available fails to give the required performance. It is unlikely that this problem will be solved all at once in the near future.

Unlike in the case of the current TV system, a sophisticated shooting method need be employed for better image reproduction. In fact, many film production methods have been incorporated in the HDTV system software development. This approach is called electrocinematography. The study on the advantages of film production technology of a long history has led to the development of a fixed focal lens with enhanced performance. Of course, a low-magnification zoom lens has been developed in parallel.

[Reduction in Running Cost]

The running cost of the present camera is very high partly because of a relatively short service life of the pickup tube. The new pickup tube is designed to last as long as tubes used in the present TV system. This means a considerable reduction in the running cost.

Autostereoscopic Three-Dimensional Television Experiment Using Lenticular Sheets and a High-Resolution Braun Tube

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I. Introduction

For realization of an autostereoscopic 3D television, it is essentially important to reduce informations to be displayed for an observer, because optical wave informations from a 3D object are too large to be handled electronically in real time.

It is an acceptable hypothesis that an image recognized by a human observer is the image which is created in his brain from data percepted by his eyes. To display a 3D image, therefore, it is sufficient if constituent data enough for a human brain to create an unambiguous image in real time are supplied. This means that informations necessary for 3D image display can be tremendously reduced, when the observer's eye lenses are included in the optical system for image reconstruction, and his inherent ability of image recognition is also included in the data processing system.

It has been shown that an autostereosopic 3D television is possible either by the volume scanning method with optical sectioning in real time or by the projection method using a lens plate. The former method has not only an inherent disadvantage of phantom image problem, but also needs a high field-frequency necessary for flickerless observation. This requirement makes it difficult to match with the already well-developed 2D television system. The latter method needs a high quality 2D display device, which must have a large display area, high resolution, good chromaticity, high brightness, and high positional accuracy necessary for registration with a lens plate, although this method is superior to the former in the compatibility with the 2D television system. 1)

2D display devices having a matrix of tiny fixed-position display elements, such as liquid crystal, electroluminescent spot, plasma glow spot, fluorescent spot, or light-emitting diode, have the accuracy for registration with a lens plate. But, they have at the present moment neither the large display area nor the high resolution, both of which a Braun tube does have.

In this paper, an autostereoscopic television experiment, using a high-resolution Braun tube with beam indeces and lenticular sheets, is described. The positional accuracy of display has been improved by the newly devised "position-synchronized-read-out method". The precise image drawn on the fluorescent screen of the tube is displaced onto the back focal plane of a lenticular sheet by means of the other newly devised "modified relay-lens plate". 3) ~ 7)

2. Experiments

Figure 1 shows a simplified diagram of the experimental apparatus for displaying an autostereoscopic-3D-television image. HRBT is a high-resolution Braun tube with beam indeces(IPS), which are fluorescent stripes (with 50μm width and 1mm pitch) printed on the thin aluminum electrode(AFE) at the back of the fluorescent screen(IDP). When IPS is hit by a dynamically focused electron beam (with 70μm spot diameter and accelerated by 20kV), it emits a light pulse (in green), which is received by 4 photomultipliers(PM1~PM4) through windows of the glass envelope of the tube. After amplification and shaping, this index signal determines the timing (in ISPG) of the read-out pulses (~5.6MHz) and the interpolation timing signal(~45MHz). Both of them determine the exact timing of reading-out (in GIRC) pixels of 8 parallax images sequentially from the memory(PIM). Thus, 8 parallax images are interleaved in registration with IPS, and simultaneously displayed at the rate of 60 3D-images per sec. (525/2 interlaced horizontal scans per 1/60 sec.) 3D video bandwidth is 30MHz.

In Fig.1, CLP is the composite lens plate, which consists of the modified relay-lens plate and the lenticular sheet(LP). Since the face plate(GP) of the tube is much thick - er than a lenticular sheet having a wide viewing zone, the image on IDP must be displaced onto the back surface of LP. The modified relay-lens plate consists of another lenticular sheet with a long-focal length and 7 masks, all of which are in registration with IPS, and it forms 8 line-images per pitch at the back of LP. These 8 line-images per lenslet of LP generate 8 fan beams. An observer at 0.7~1.5m in front of LP chooses arbitrarily two of those beams at a moment with his eye lenses, and then he recognizes naturally a 3D object in real time.

Figure 2 shows a photograph of the experimental Braun tube with the composite lens plate. Figure 3 shows stereo-pair photographs of a reconstructed 3D image of a plasticine statue. The parallax images of this 3D image were taken by a CCD camera with the object on a rotating table. The display area has 280mm and 220mm in the horizontal and vertical directions respectively, and the lateral and logitudinal resolutions in

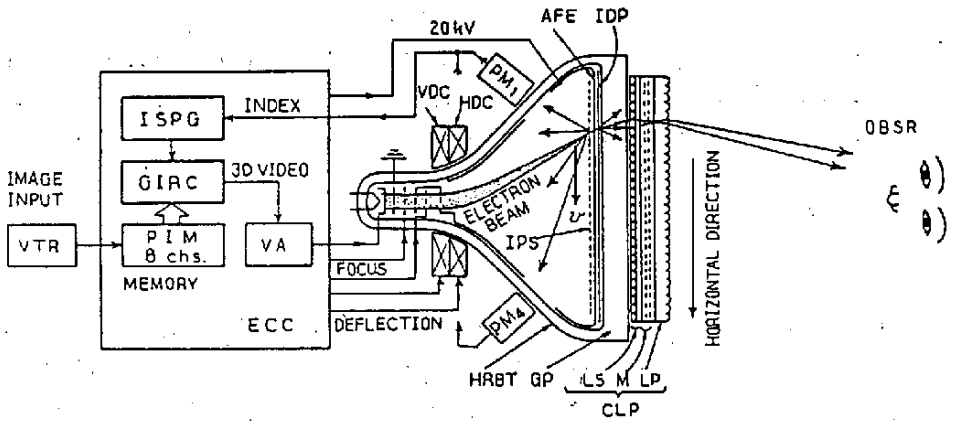

Figure 1. Simplified diagram of autostereoscopic 3D television display

the vicinity of LP are 1mm and 16mm, respectively. The viewing zone has approximately 20cm width. The image brightness and the width of viewing zone can be improved if LP is contained in the tube's envelope.

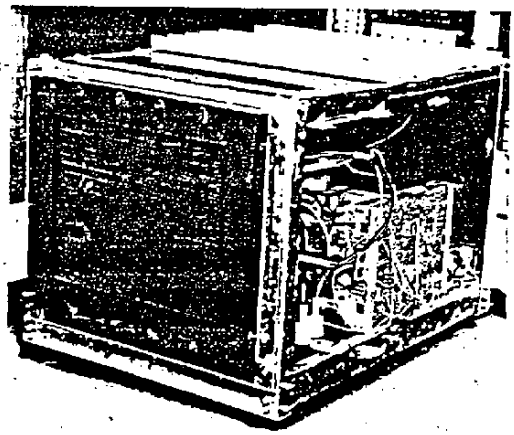

Figure 2. Experimental Braun tube with the composite lens plate

3. Discussions

3.1 Stabilization of the index signal

When a high-resolution Braun tube with beam indeces is the device of displaying a 3D image, accurate read-out pulses must be generated even if 3D video signal is strongly amplitude-modulated.

Focusing and deflection-linearity of a Braun tube at the begining of a horizontal scan are generally poor, and the first index stripe is not always expected to be usable for determining the start pulse. Therefore, to generate the start pulse of displaying in each of horizontal scans, deflection linearity at the starting position of displaying must be adjusted within a certain tolerance, and an index stripe without defects along its full vertical length must be found out and be used.

Because 3D video signal having depth informations is deeply and quickly changing, it is necessary to superpose a video pulse with a constant amplitde for establishing the start pulse. And it is also necessary to use a phase-lock-loop(PLL) for stabilizing the read-out pulses for each of horizontal scans. Moreover, phase shift of index signal at amplification and PLL(in ISPG shown in Fig.1) must be minimized, since index pulses are not periodical at all. To reduce disturbances due to transient phenomena in ISPG, it is often effective to superpose short video pulses, which are synchronized with the read-out pulses and at the phase to hit the index stripes. These auxiliary

Figure 3. Stereo-pair of a 3D image reconstructed on the Braun tube

pulses are superposed on the 3D video channel in VA shown in Fig.1

3.2 Autostereoscopic 3D television camera

Since television camera devices have resolution poorer than a high-resolution Braun tube, a necessary number of parallax images must be taken with many optically aligned cameras. CCD(charge-coupled-device) camera is one of the best for this purpose, because it is compact in size, and has positionally fixed photoelectronic-conversion elements with high sensitivity.

For adjusting magnification and distance, the same method as an autostereoscopic 3D camera is applicable. If a television camera with very high resolution become available, a single camera device with the same optics as the 3D camera would be usable. 2)

4. Conclusions

It has been demonstrated that an autostereoscopic television display is done by using a high-resolution Braun tube with beam indeces.

Although stereoscopic television systems are already in market, many important subjects are left unsolved in the field of the autostereoscopic 3D television. Some of them are listed as follows:

1) Full color autostereoscopic television
2) Autostereoscopic television with a wide screen and high brightness
3) Frequency-band reduction of autostereoscopic television signal
4) Compatibility with the 2D television system, including apparatus for recording
5) Standardization of autostereoscopic television system

For future development of autostereoscopic television system, mutual colaboration between people in the fields of electronics, vision research, information processing and many application fields of 3D television is strongly needed.

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3DTV WITHOUT GLASSES

Reinhard Börner

At Heinrich-Hertz-Institut in Berlin/West-Germany the author is developing 3-D-System for projection onto lenticular screens.
The diagonal of the large screen and the viewing distance are of about the same length in order to obtain a most natural impression of presented space and objects.
Using sidelobes of parallax panoramagrams for projection, the distance between the projectors (e.g. 6 projectors for 5 stereopairs) is no longer limited to the spacing of the observer's eyes. Therefore no special projectors are required; customary projection equipment for slides and video may be used.
On the other hand, the selectivity of a wide-angle lenticular screen has to be increased enormously to minimize crosstalk in the outer panorama zones. This was achieved by a certain arrangement of the projectors, and by a new type of optical correction with increased selectivity across the whole area of the screen and throughout all viewing-zones.
The photographic projection equipment was introduced for the first time at Funkausstellung in Berlin 1986 and in addition a monocromatic recording- and projection system at HDTV-Kongreß in München 1987. This equipment will be explained and some aspects of future application to video camera and projection system will be discussed.

6. コンピュータ分科会アブストラクト

6. コンピュータ分科会アブストラクト

Data Base Machine Architectures

H. O. Leilich

Abstract:

Data Base Management Systems made significant progress in the last decades due to hardware availability (especially inexpensive mass memories), along with the maturing of mathematical concepts and software engineering (relational model, transaction concept, fault tolerance). General purpose computer systems are inefficient in performing rather simple operations (searching and sorting) on large amounts of data as well as memory management. Users of DBMS's require high transaction rates, dependable permament service, and data security rather than the full flexibility of a universal computer system. Thus special purpose back-end systems (Data Base Machines) have been devised, which ought to adapt available hardware and software such that system requirements are fullfilled in a more efficient way. In the changing world of hardware and software technology along with moving system requirements, no new universal architecture has been broadly accepted by the market so far.

Our institute has actively participated for many years in the world-wide research toward such an architecture. Complete hard- and software models have been built and evaluated (SURE, RDBM, IDC).

Another field of activities in our institute is the conception, design and test of special computers for space research (e.g. for the Japanese mission "Geotail"), where fault-tolerance is a prime requirement.

Research Activities on Fault-Tolerant Systems in Japan

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1. Introduction

In 1980, the 10th International Symposium on Fault-Tolerant Computing was held in Kyoto, Japan. Since then, the ad hoc committee on fault-tolerant computing was organized in the Institute of Electronics and Communication Engineers of Japan (currently Institute of Electronics, Information and Communication Engineers - IEICE) to spur research activities on fault-tolerant systems. Later, this committee was expanded to Technical Committee on Fault-Tolerant Systems (TCFTS), IEICE in 1986. This TCFTS sponsors regular technical meetings four times each year, in addition to session(s) and/or symposium on fault-tolerant systems at annual National Convention of IEICE. Further, the informal workshop is held two times a year. The Ministry of International Trade and Industry (MITI) started a survey committee on fault tolerant computing technologies in 1982.

Theory and techniques on fault-tolerant systems have been taught as a course in the graduate program at Tokyo Institute of Technology since the early 1970's and the similar course(s) will be opened soon at other Japanese universities.

Due to these organizational supports and individual efforts, many original as well as developmental contributions have been made in Japan to fault-tolerant computing technologies. They include Theory of Fail-Safe Systems, Applications of Error- Detecting/Correcting Codes, Test Generation Algorithms, Testability Design, System Architectures, and Software Reliability Evaluation. A part of them has been reported at Baden Symposium on "Evolution of Fault-Tolerant Computing" in 1986, which was sponsored by IFIP WG 10.4 [1]. The aim of this paper is to supplement the previous report with an emphasis on researches conducted mainly at universities and national research laboratories in recent years. Industrial development of fault-tolerant systems will be reported elsewhere.

2. Design of Totally Self-Checking Circuits

As A. Avizienis pointed out at the seminar in Frankfurt [2], the first step of fault tolerance is the detection of fault(s) in the system. The combination of a totally self-checking (TSC) functional unit and a TSC checker is capable of detecting fault(s) "on-line" not only in the functional unit but also in the checker itself, and thus the realization of TSC checkers attracts much attention these days. The significance of TSC approach will become greater in the VLSI implementation of super- parallel processors and/or the data-flow mechanism [3],[4].

Among error-detecting codes is used the 1-out-of-n code in, say, address decoder circuits. Anderson and Metze already showed the way of constructing TSC checkers for this code with 4 or 5 logic levels [5]. (This scheme is actually implemented in the microprogrammed control circuit of Bell's No.3A ESS (Electronic Switching System) [6].) In contrast, Izawa proposed new design of TSC 1-out-of-n ($n > 3$) code checkers which needs only 3 logic levels [7]. The characteristic structure of his design is as follows. The set of n outputs of OR gates at the second logic level (from the primary output of the checker) represents (n-1)- out-of-n code instead of 1-out-of-n code, where these n outputs are divided into two groups to feed two AND gates at the first logic level, respectively. The outputs of these two AND gates obviously represents 1-out-of-2 code, contributing to the fault- secure property and the code-disjointness. Further, he provided at the third logic level a column of OR gates (called the shared gates) of n-2 primary inputs. Each output of these shared OR gate at the third logic level was used to supplement n-2 inputs to the OR gates at the second logic level and more importantly shared by OR gates of different subgroups for two AND gates. (If we feed each OR gate simply with n-1 primary

inputs, the self-testing property for an input at these OR gates is not guaranteed.)

His idea can be extended to TSC m-out-of-n code checkers [8]. By applying Anderson and Metze's idea of TSC k-out-of-2k code checkers to m-out-of-n code checkers and simply decomposing the circuit structure based on the threshold logic into a two- level AND-OR form, the self-testing property for an input of AND gates cannot be realized. Then, we provide the circuit with the third level of the shared AND gates as in Izawa's case.

The realization of microprocessors with TSC/SFS property is one of challenging issues [9]-[11]. Nanya and Kawamura has designed Strongly-Fault-Secure (SFS) version of i8080 microprocessor [12]. They used the two-rail code in ALU section (this means 16-bit in stead of 8-bit accumulator was used for 8- bit data), Berger code in registers with 4 check bits for 8-bit data, and in the control and sequencer section as well with 6 check bits for 57-bit data. The overhead of their design in terms of gate counts was 38%. The area overhead of TSC microprocessors could be ignored with the progress of integration technology. However, more logic levels required for Berger code checkers, as an example, may prevent the use of higher rate of the clock signal, thus degrading the operational performance of the microprocessor. Therefore, the incorporation of TSC/SFS mechanism into microprocessors may still need further improvement in the design of TSC checkers.

3. Testability Design

The increase of circuit complexity has made it very difficult to test VLSI circuits even "off-line". To alleviate this difficulty, the use of extra hardware to ease the test is now becoming common and of realistic value.

PLA has rather unified structure suitable for VLSI implementation of logic functions. In 1980, Fujiwara et al showed a way of constructing PLA [13], for which the test can be applied independently of its function. Their basic idea is to add extra lines to AND and OR arrays for encoding these two arrays into parity check code. The PLA also has a shift register to activate each product line individually, modified input decoders to activate each primary input lines individually, and chains of EX-OR gate to check the parities on AND and OR arrays. The function-independent test mainly consists of the sequence of activation of each of primary input and product lines.

It was a surprising coincidence that the similar idea was also proposed by Hong et al at the same Symposium [14].

The PLA above includes rather heterogeneous structure for the shift register and may suffer considerable area penalty, as E. McCluskey pointed out. The incorporation of a specific PLA structure to control the activation of product lines was proposed by Sato and Tohma [15]. The similar approach is being pursued by a group at Stanford [16]. Saluja et al's idea [17] is interesting in the sense that their PLA structure does not use even the chains of EX-OR gates. The test of their PLA, however, is no longer function-independent.

The Built-In Self-Test (BIST) is certainly an effective approach to testability design. Since BIST relies on (pseudo) random testing, an issues will be raised on how much we can be confident of fault-freeness after the completion of successful test. Wakimura and Tohma evaluated that even after the application of 2**n random inputs to a n-input combinational circuit with no indication of errors, we could be about 70% confident of the normality of the circuit [18]. Furuya also made the similar evaluation from the point of view of exhaustive testing [19].

Other many topics concerning BIST as well as the excellent test generation algorithm given by H. Fujiwara are described in [1].

4. Knowledge-Based Approach

Logical inference with a knowledge base is one of features of recent computational techniques. The knowledge-based approach to testability design was already presented at FTCS-14 [20].

Kameyama et al applied a knowledge-based technique to control inlet valve A1 and outlet valve A2 for reserving water in a tank within a predetermined limit [21]. The control conditions are represented as a set of rules like

(1) IF 0 < t1 < tl1 THEN A1 is open and A2 is closed

(2) IF th1 < t1 THEN A1 is closed and A2 is open

(3) IF 0 < t2 < tl2 THEN A1 is closed and A2 is open

(4) IF th2 < t2 THEN A1 is open and A2 is closed

where t1 and t2 are elapsing times during the increase and decrease of water in the tank, respectively. tl1 (tl2) and th1 (th2) are the expected minimum and maximum elapsing times of the increase (decrease) of water, respectively. The abnormality can be detected as some of the above rules is violated.

The unification of Prolog can be viewed as the bidirectional implication. This property is surely useful for determining the test input of combinational logic circuits. Further, The ease of representing facts and rules is likely well exploited in modular approach to very large complicated circuits. Thus, we can be benefited by the concise formalism of Prolog.

However, the execution of Prolog programs on currently existing machines is not necessarily very efficient. Goto and Tohma [22] showed that the execution of Prolog programs for test generation could be well accelerated by specifying the area where the four-valued simulation should be performed. Unnecessary backtracking is avoided in this way. The possibility of improving performance by the adaptive placement of facts and rules was argued by Varma and Tohma [23].

5. Fault-Tolerant Systems

The construction of real fault-tolerant system and its application to railway interlocking systems has been conducted at Railway Technical Research Institute, Japan National Railway (this organization has been recently changed to a non- governmental institution) [24]. The most critical part of this system is constructed in triple modular redundancy and by using specially designed fail-safe logic components. The principle of the fail-safe component is to use the oscillation and its cease to represent logic values 1 and 0, respectively. When a fault occurs, the circuit structure forces the oscillation to cease immediately [25].

An experimental SIFT-like loosely synchronized TMR system, of which nickname is SAFE (Software Assisted Fault-tolerant Experimental) system, was constructed at Tokyo Institute of Technology [26]. The synchronization mechanism for interrupt handling under the environment of loosely synchronized TMR systems was investigated [27].

When simultaneous (or correlated) errors are caused at multiple processing units by, say, external noise, TMR systems with rather tight synchronization do not work well. To avoid this simultaneous disturbance, the microcomputer-based TMR system constructed at Tohoku University used the time skew. That is, the same operation is carried out in different time slots at different processing units [28].

Distributed and/or autonomous processing are attracting attentions even in terms of fault tolerance. A packet-relaying mechanism called the container concept, by which triplicated packets are transmitted thrpugh three disjoint paths and the majority-vote of them is taken at the destination node, has been proposed [29]. Other topics such as the incorporation of fault tolerance into data-flow mechanism and distributed databases as well are now investigated at Tokyo Institute of Technology.

6. Software Reliability

In the realization of highly reliable computer systems, no one can ignore the significance of software reliability. Recent survey conducted in Japan revealed that about 26% of causes of system down was due to software faults [30].

Software reliability may be evaluated by:

(1) Error rate in service operation

(2) Percentage of tested paths to all possible ones of a program

(3) Estimate for the number of residual software faults

Researches on (1) are few in Japan, while a new measure of the coverage in terms of (2) was proposed by Chusho [31]. Osaki et al at Hiroshima Univ, Okayama Univ of Science, and Japan IBM are pursuing (3), using models based on the Non-Homogeneous Poisson Process (NHPP) [32],[33]. While the NHPP model was

first introduced by Goel and Okumoto [34], they modified the average function to reflect the s-shaped behavior commonly observed in the growth curve of the cumulative number of detected software faults. Tohma et al recently proposed a model of (3) based on the hyper-geometric distribution [35]. They claims that the structure of software can be taken into account in their model. Further, they consider the effects of test items as well as the increase of skill in the test [36].

7. Conclusion

Researches on fault-tolerant systems conducted mainly at Japanese universities and national research laboratories have been surveyed briefly. It should be emphasized that there are many other researches not included in this paper, since this paper is not necessarily intended to make a complete survey. Next year the 18th International Symposium on Fault-Tolerant Computing will be held in Tokyo, where, we hope, many results of current researches not only in basic area but also in applications will be presented.

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Realization of Fault-Tolerance
- Autonomous Decentralized System -

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Most large scale and real-time control systems have three major characteristic requirements. The first is that the system can continue its operation through the fault occurrence in it, lest the unexpected shut down of the system should result in serious damage. The second is that the system is gradually constructed step by step and at any step the part of the system can start its operation even under the construction of the other part. The third is that the failed part of the system can be repaired during the operation of the system.

These needs imply that the large scale control system has three intrinsic requirements of fault tolerance, extensibility and maintainability. These three requirements cannot completely be satisfied in the centralized system and even in the conventional decentralized system.

A new design philosophy for autonomous decentralized control system, based on a biological analogy, has been developed for structuring and controlling a distributed system which satisfies the aforementioned three requirements since 1977.

In molecular biology, which has recently made enormous progress, a living thing is viewed not as a whole unit but as a set of cells. The fundamental concept is that a cell intrinsically has all the genes necessary for its growth.

Cells are fundamental living subsystems having the same structure and the same information. Although there are no supervisory elements to control them integrally, those independent cells collectively perform the function of organs.

We have grasped a biological organism as a system with the following attributes.

(1) The system always has faulty parts;

(2) It changes constantly, alternating between operation, maintenance, and growth; and

(3) It keeps accomplishing its objective almost completely.

Our concept has been introduced by this biological analogy, that is, a living thing is always renewed by metabolism and gradual growth. Therefore, it is quite normal for a system to have failed parts, in other words being faulty is normal.

Subsystems are not considered to be parts of a divided total system, and are considered to be required the following three properties: (1) Autonomous Observability (2) Autonomous Controllability and (3) Autonomous Coordinability.

Autonomous Decentralized System (ADS) requires the constituent subsystems to have the following three conditions: (1) Uniformity (2) Equality and (3) Locality.

The system control and coordination of ADS are explained in Fig. 1.

Those properties suggest that the ADS structure is an aggregation of homogeneous, uniform subsystems, each having intelligence — with hardware and software systems not in the master-slave relation — and each being equivalent in capacity and performance.

The information system in ADS can be summarized as follows:

(1) There is no priority given to any information or transmission.

(2) All information is transmitted consecutively to the subsystems adjoining to the generating point. Each subsystem picks up what it needs from the transmitted information and transmits all information to the adjoining subsystems.

They suggest that every subsystem requires an intelligence to manage itself and to coordinate with other subsystems. That is, the software subsystem consists of not only the application modules but also its own management module, which is called the ACP (autonomous decentralized control processor).

For communicating and coordinating among the subsystems without using the common file, the data field (DF) concept is proposed.

The content code protocol is used. The content code indicates the meaning of the data. Every item of data attaching its corresponding content code is broadcast into the DF and it is selected to be received by the ACP.

Some of the subsystems which consist ADS are shown.

The autonomous decentralized loop (ADL) is a system constituting

a subsystem that is positioned at the same level as other subsystems. As shown in Fig. 2, it has a double-loop structure designed for optical transmission in opposite directions. The network control processor (NCP) is a controller that controls the transmission line. Two NCPs in each loop are fused and connected to a host processor. The length of communication can be selected arbitrarily. In addition, the NCP has a built-in tester and is identical for both hardware and software; the software (stored in the ROM) is used for transmission control.

Detection, removal, and recovery of faults in the transmission line are performed independently by each NCP. Each NCP checks the line to determine the possibility of transmitting to neighboring NCPs and selects a bypass if the transmission is not possible.

The fault-tolerant multi-microprocessor system based on the autonomous decentralized system properties is designed as an aggregate of microprocessors whose homogenous structure and autonomous functions suggest organic cell. The cells, which connected in a hexagonal shape (see Fig.3) by the fault-tolerant bus (FTB) have the same characteristics as the ADL. The FTB, however, provides bidirectional gates for each cell. Gates are controlled by the cell. When an FTB fault is detected by the adjoining cell, the gate of that cell is opened and no information is transmitted further to cells. Each cell is connected with the three-way FTB and information generated in the cell is immediately and consecutively broadcast to the three FTBs.

This system constitutes a fault-tolerant structure; its functional reliability is assured by task distributions. While each cell executes one or more tasks, several cells are instructed to execute the same tasks and the results are fetched for checking by other cells. By so doing, (n-r) out of n can be selected — according to the importance of the task — by majority voting or threshold-voting.

On-line maintenance is provided by two components: the Built-In Tester, or BIT, which is installed in every subsystem for subsystem-level maintenance support, and the External Tester, or EXT, which integrates the BIT's information for system-level maintenance support.

This autonomous decentralized control system concept is still in the research stage, but has been applied in various systems to control trains, multistage dams, water supply production, iron and steel making

process and so on. The realization of this new concept is not so rapidly accepted because of compromise with the already-accepted technologies, however, some of idea, mentioned above, are step by step applied to the computer systems.

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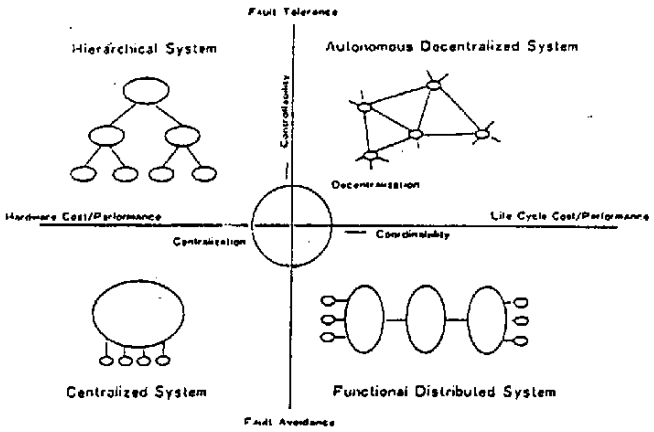

Fig.1. System classification

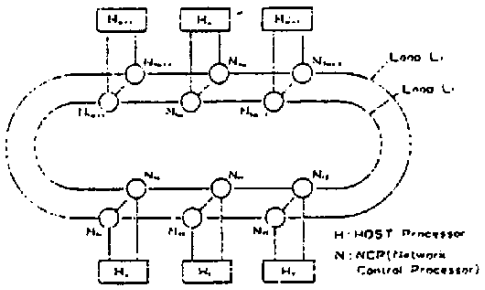

Fig.2. System structure of autonomous decentralized loop network

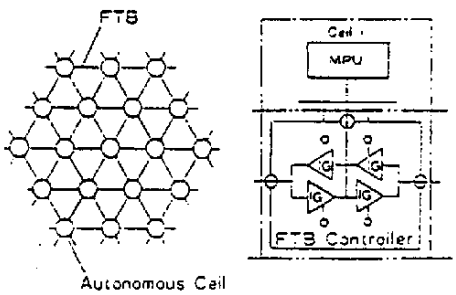

Fig.3. System structure of autonomous decentralized multi-micro processor

Synopsis of Lecture

Fault-Tolerance by Synchronisation of Real-Time Task Systems on Multiprocessor Duplex Computers

H. Meyerhoff, Krupp Atlas Elektronik

In many fields of process automation, high requirements are imposed regarding the reliability of data acquisition and data storage.

- Input data must not be lost: they cannot be repeated.

- Stored data must be consistent and must be stored safely.

These requirements can only be fulfilled by a computer system which

- has a fault-tolerant design in all parts and

- is available continuously. "Cold stand-by" or "roll-back" methods are ruled out.

At Krupp Atlas Elektronik, a computer system has been developed for these requirements.

The system is composed of two linked multiprocessor computers of the type MPR 1300.

Each MPR 1300 consists of up to eight parallel, equal-priority processors which access shared memories via four parallel buses.

The distribution of the tasks among the processors is performed dynamically in a priority-controlled manner during the actual run-time.

The software system is executed in the same way on both linked multiprocessor computers. Both computers access the same data and output the same data; the data output of one of the computers is physically blocked. If one computer fails, the process carries on running in a trouble-free manner, without any discontinuity.

The identical execution of the programs is produced by synchronisation in the case of particular machine-instructions (mainly tasking instructions and input/output).

The method of synchronisation of task systems in a real-time environment (e.g. interrupts) is described in detail in the lecture. The same applies to the method of monitoring the synchronisation. The instructions which are used for synchronisation are privileged instructions (with one exception, which is described), i.e. they are used in system programs only.

User programs are not affected by this. They can therefore be executed in unmodified form both on the single MPR 1300 computer and on the MPR 1300-SD duplex computer.

DELTA-4: The European Research Project for an Open, Fault-Tolerant Multicomputer Architecture

by

Peter M. Behr

Abstract:

DELTA-4 is an ESPRIT-funded research project for the Design and Development of an Dependable Distributed system architecture. The aim of the project is to enable modular system configurations offering a range of performance and dependability in an open, distributed environment. Target applications of the DELTA-4 architecture are mainly in the fields of Office Systems and Computer Integrated Manufacturing, but also Process Control Systems and Transaction Processing Systems will be supported.

Network management and the protocols for inter-process communication are designed to be conform to existing or evolving communication standards. DELTA-4 will also influence further standardizations by making proposals for necessary extensions to achieve the required degree of dependability and performance. With respect to the dependability and real-time requirements the technical goals of DELTA-4 are far beyond the aims of the well-known MAP project.

In support of this objectives, DELTA-4 defines an abstract language-independent, computational model for the construction of dependable distributed systems. The management of the distributed and fault-tolerant aspects of the systems will be transparent to the programmers.

The presentation covers the organizational and the technical aspects of this ambitious project. The overall structure of a DELTA-4 system will be described and some of the main technical solutions will be discussed.

Rapid innovation in industrial automation, a challenge for software engineering

W. Howein

(Siemens AG)

Software development in industrial automation has to take place under hard conditions: competitive products and systems require rapid innovation. On the other hand, competetivness of software development needs long-lived tools independent of product and system innovation. Otherwise the software tools would have to follow closely the innovation cycles of its targets. This would cause prohibitive costs and schedule-overruns. The industrial approach to these problems constits of software factories with well definded software engineering principles, a powerfull software engineering workbench and appropriate organisations. This allows a well defined work-sharing and an increase of productivity.

The key concept of the software engineering workbench is a host target approach with only one tool set for different dedicated automation systems. A network of personal computers and engineering workstations is the software engineering host to the existing automation systems. The software workbench is based on UNIX. Chaining of tools allows pipelining from requirement analysis to automated coding and testing. The tool set is connected to a configuration management and documentation system. Libraries with modules for systems and technologies stimulate the reuse of software. Reusable software and powerfull tools are the two basic elements of the increasing software engineering productivity in our company.

The evolution of automation technologies and software engineering techniques leads to the design of larger plants with higher complexity and more distribution with many different interfaces. The handling of knowledge, that means knowledge aquisition, -representation and -retrieval will become a key roll in our future software engineering workbench.

Research and Development Trends on Automating the Software Production in JAPAN

Shuetsu HANATA

NTT Software Laboratories

Research and development on automating the software production are now under way in many organizations of JAPAN. These automatic program synthesis technologies can be divided into the following four approaches.

(Type 1) Theorem proving
An approach to synthesis of a program, by theorem proving, from a given specification which is composed of logical relations between input and output conditions.

(Type 2) Synthesis from examples
An approach to synthesis of a program from examples by inductive inference.

(Type 3) Synthesis from high level description
An approach to synthesis of a program from high level specification or program descriptions through program transformation. This can be further divided into three approaches depending on input description styles:
-formal specification description approach
-high level program description approach
-natural language specification description approach

(Type 4) Reusing program components
An approach to synthesis of a program by combining program components into a target program which satisfies its specification.

In these, the approaches of types 1, 2, 3 are generally at research level, while the type 4 approach is at partially practical level, especially in the business application area. The following table and figures show the trends on automatic software production technologies in JAPAN and two examples, SDE[1] and TELL[2] belonging to the type 3 approach. SDE is a design and maintenance environment for communication software, which supports the automatic renewal of existing software to meet new service specifications with protocol verification and synthesis techniques. TELL is a natural language based software development system which provides natural language interface and semantical processing functions.

In JAPAN, improvement in software productivity is being achieved by the type 4 approach. This approach will expand its application area as a result of its refinement brought about by actual use of the approach. As a next stage, the type 3 approach will be partially applied to some limited areas such as the banking application software in a couple of years.

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[2] H.Enomoto, N.Yonezaki and S.Saeki, "Natural Language Based Software Development System TELL", Proc. of ECAI-84, Pisa 1984

Table 1 Automatic Software Production Technologies in JAPAN

Type of Approaches		Organization	System
1.Synthesis of program based on theorem proving		She,A.(Kyoto Sangyo University)	
2.Synthesis of program from examples		Nakajima,H.(Kyoto University) Arikawa,S.(Kyusyu University)	
3.Synthesis of program from high level description	from formal specification	Ito,T.(Tohoku University) Agusa,K.(Kyoto University) Noguchi,S.(Tohoku University) Katayama,T.(Tokyo Institute of Technology) Inagaki,Y.(Nagoya University) Taniguchi,K.(Osaka University) Ichikawa,H.(NTT)	SDE
	from high level program	Tamaki,H.(Ibaraki University) Torii,K.(Osaka University)	
	from natural language	Uehara, K.(Osaka University) Yonezaki,N.(Tokyo Institute of Technology)	TELL
4.Synthesis of program by reusing program components		Kuse,K.(Tsukuba University) Nisida,F.(Osaka Prefecture University) Matsumoto,M.(NEC) Tsuda,M.(HITACHI) Nisino,H.(FUJITSU) Harada,M.(Central Research Institute of Electric Power Industry)	SEA/I EAGLE MASCOT SPACE

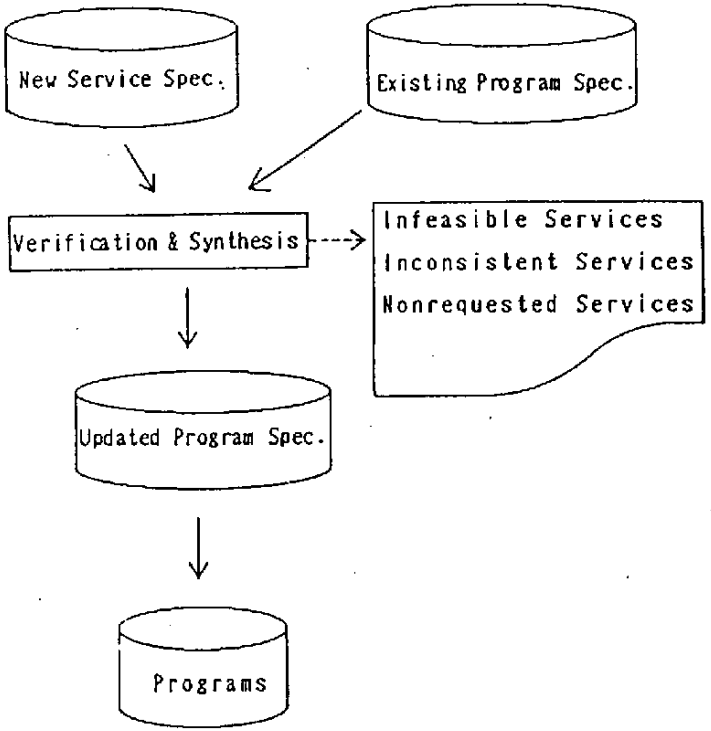

Fig.1 Specification Descriptions and Their Operation in SDE

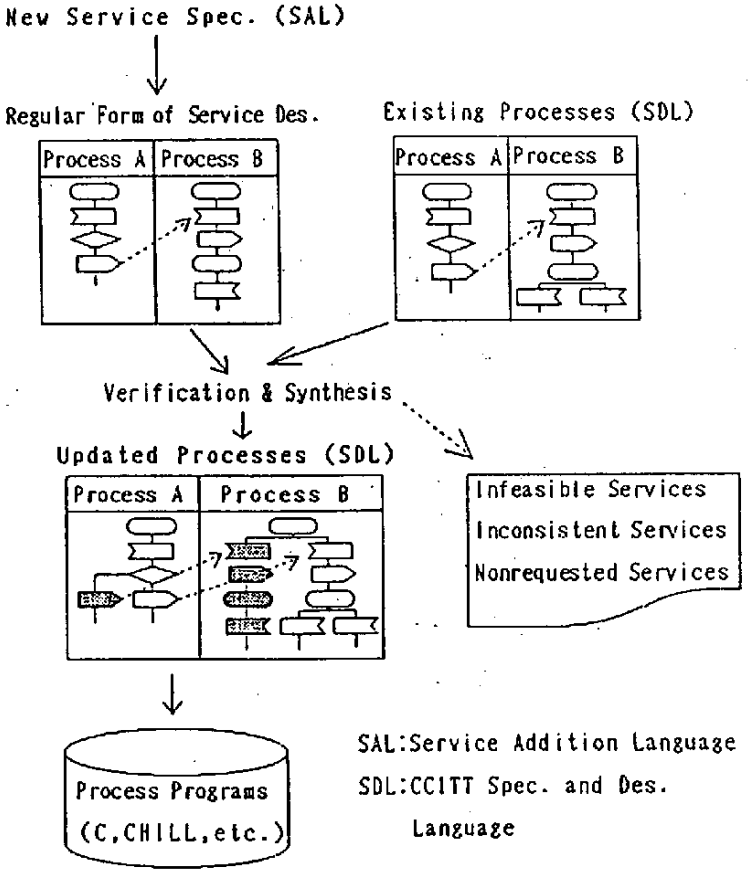

Fig.2 Specification Descriptions and Their Operation in SDE

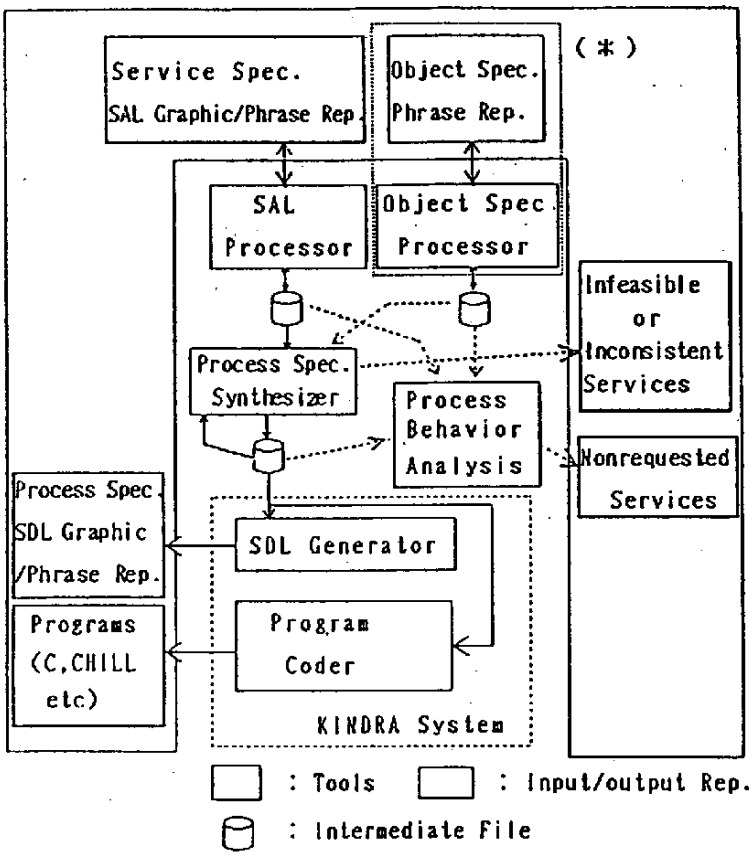

Fig.3 Communications Software
Design and Maintenance Environment SDE

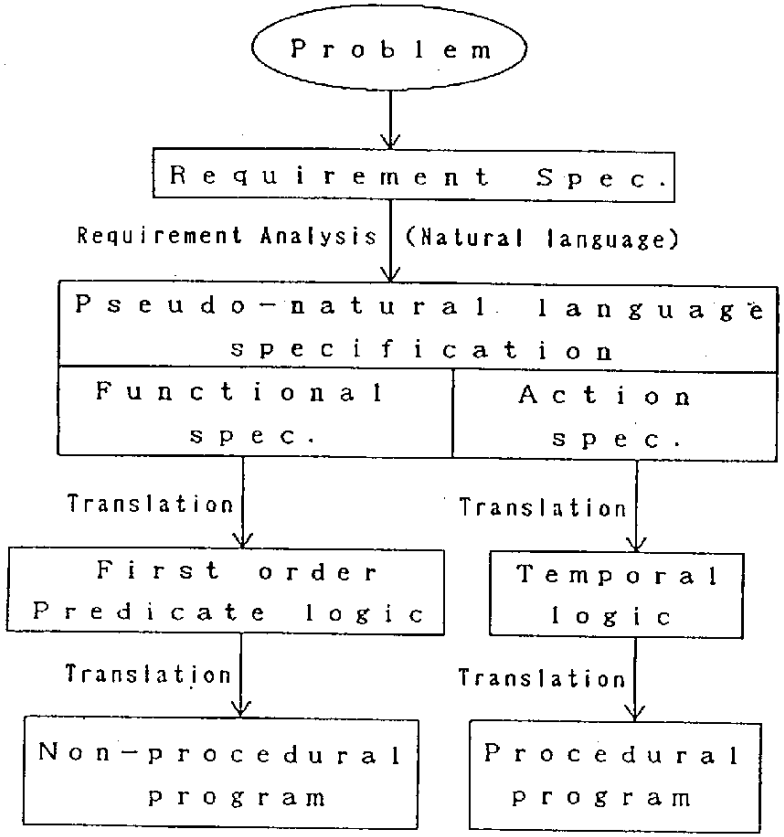

Fig.4 Natural language approach in TELL

```
Pages T is pagenated from file F between minimum line number Min
  and maximum line number Max means that
   case 1) F.is empty: T is empty.
   case 2) F is not empty:
         2-1) The result of separating a page from F is
              page P and file F1.
         2-2) Pages T1 is pagenated from F1 between Min and Max.
         2-3) T is the concatenation of P and T1.
  The result of separating a page from file F is page P
    and file F1 means that
     1) Line number N is the next important in F from Min+1 to Max+1.
     2) The result of breaking F at line number N is P and F1.
    The result of breaking file F at line number N is
      file F1 and file F2 means that
       1) F1 is the first half sequence of F with line number N-1.
       2) F2 is the last half sequence of F with line number N.
    end break;
  end separate a page;
                    .
                    .
                    .
end pagenated;
Number is positive integer.
Line number is positive integer;
Pages is sequence of page.
Page is file.
Line is sequence of character associated with tail.
   Line L1 is the tail of line L means that
         1) L is the concatenation of character C and line L1.
   end tail;
end line;
                    .
                    .
                    .
lexicon
Minimum line number := line number.
Maximum line number := line number.
Blank line := empty.
                    .
                    .
```

Fig.5 Example of specification written in TELL

An Overview of Software Engineering Architecture/One (SEA/I)

NEC Corporation

M. Matsumoto

1. Introduction

Today, software productivity and quality control is becoming extremely important in an in an increasing number of fields. Current businesses, in which information management plays a leading role, strongly requires realization os software engineering architectures and CASE (Computer-Aided Software Engineering) systems through which quality software can e and cost restrictions.

This short paper describes SEA/I (Software Engineering Architecture/ONE) as a typical CASE system example.

2. The SEA/I outline

The SEA/I allows developers to have the image-based prototyping and system/program design. The SEA/I provides the automatic program generation and synthesis functions by which a target system is produced efficiently along with the design results.

The SEA/I also allows developers to have an easy way of reusing the existing software resources. work results phase. One systemdevelopment achievements are horizontally re-utilized upon another system development occasion. All the SEA/I production facilities and software resources integrated into a set of production system and to support target system's total life cycle. This is a reason why the SEA/I is thought one of the most powerful development systems. The noteworthy points of the SEA/I are summarized as:

(1) Visualization-based design

This design methodologies and the supporting tool system allows developers to have integral aspects of software design based on its external visibilities: (1) the form image design method is for interactive screen, output reports and file form design, (2) the Entity-Relationship model based system structure design method is for defining and refining of a system hierarchical structure and is for specifying a usage relationship of forms among system components, and (3) the tree diagrammed program structure design method is the appropriate way to obtain a structured program.

(2) Automatic Program Synthesis

The visualization-based design output is in turn transformed into source- level program parts by the SEA/I Parts Generator. These program parts are automatically synthesized into a complete program that is consistent with the design specification.

(3) Software Reusability Management

The object visualization programming method allows developers to appropriately make a judgement on whether or not a certain existing software resource is reusable, and in case of reuse with changes, allows to modify in ease. Software resources are stored and managed under the data dictionary/directory services, so that one is able to access the necessary resource promptly.

(4) Total Life Cycle Support

The Sea/I is a comprehensive software productivity system providing the automatic set-up functions of test and production run environments, the maintenance support

and the documentation generator as well as upper work phases supporting capabilities.

3. Conclusion

The SEA/I gives user many advantages as :

- easy to compare requirements with the system to be implemented, because of the rapid prototyping capabilities,

- obtained increased design and software quality and improved productivity, because of the SEA/I software CAD and CAM capabilities,

- became able to precisely build up program, because of program synthesizing capability,

- productiveness intesting a program and in installing a quality assuranced system, because of the SEA/I test and install aids.

Some of productivity improvement data measured in field are as: PROTOS and Software CAD facilities allows user to have improved systems engineers' productivity five t fifty times as much as manual work for designing data layout structures.

Misunderstandings are less conceivable among people concerned, because no need of transforming software information among work phases, but the SEA/I manages information reposit and passing. At requirements definition and designing phases, but the SEA/I manages information reposit and passing. At requirements definition and designing phases, less misconceptions exist among

developers and customers because they are able to communicate each other looking at the realistic "blue print" of the system to be implemented. These aspects of the SEA/I system are of importance with improving software quality.

FRAMEWORK APPROACH TO INTEGRATED TOOLSETS FOR SOFTWARE ENGINEERING

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The economic development of high quality computer software systems requires the application of computer based tools supporting the different domains and phases of the development process. The efficiency of software development can be increased substantially by integrating those tools, i.e. changing "tool boxes" into "tool sets". In a tool set, the information transfer and transformation between tools for different domains and of different design approaches is directed and supported through specific tool set functions and "meta-tools". In addition, a tool set provides user guidance to the development tools and through the development process. This approach helps turning the art of programming into software engineering.

Many domains and phases of software engineering are today covered by tools. These existing tools have been developed on the basis of certain design philosophies or methods; they live in their specific world and are frequently not compatible to other tools for adjacent steps in the course of software development. But considering the efforts for the development of those tools and the training of their users, it is only reasonable to integrate these existing tools rather than to develop new tools for tool sets under a uniform methodology.

The integration of tools should consider three interfaces between a tool and its environment: the input interface, where the results of the previous step of the software development process are entered; the output interface, providing the results of tool functions; and the user/system interface to execute and utilize a tool. An integration of different tools requires the adaptation of these interfaces which could be provided individually for pairs of tools, resulting in substantial costs and in

a variety of user surfaces. The current approach to integrated tool sets therefore employs standardized interface formats. All tools must be adapted to these formats either by changing their existing interfaces or by introducing interface adaptation modules for each tool. The advantage of this approach is the possibility of arbitrary combination of tools in a tool set after this adaptation has been implemented once for each tool.

The standardized interfaces and the supporting meta-tools can be regarded as a framework for adapted tools to be plugged in. Because of the complex requirements of such interfaces due to the semantic differences of tool functions and results, different standards have been developed, being evaluated world-wide in a number of software engineering projects. The mentioned above input and output interfaces are usually combined to a "data handling interface" (DHI) whereas the user interface (UI) remains as an interface of its own. The system interface is mainly determined by the operating systems for the operation of the software engineering tool set.

The DHI design considerations are governed by the kind of software system modelling. The unterlying models vary from pure trees to general entity relationship concepts. Different approaches will be introduced and discussed, considering the German joint national projects on software engineering as well as the European PCTE development and the US approach called CAIS.

The UI design considers modern work station windowing techniques and the multitasking capabilities of the operating system which is mainly UNIX. UI proposals comprise meta_tools for the definition of dialogs as well as graphic and alphanumeric input/output functions. Some currently available concepts will be presented.

The availability of integrated tool sets and the exchangibility of tools in frameworks will substantially increase software productivity. The current world-wide work towards standardized tool interfaces underlines this perspective.

The Evolution in Structured Methodologies
Achievements in Methods and Tools

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After teaching software engineering principles for several years GEI set out to develop method based tools in the early 80's. A pragmatic software and system engineering environment - called ProMod - is the result. ProMod is currently used not only within GEI, but in about 500 locations in Europe and the U.S.

ProMod is methodology based. Contrasting it with very useful general purpose utilities and tools our intention was to select industry proven methods and introduce them as foundation for goal oriented project work. This presentation explores the methodology background of ProMod, showing how Structured Methods have evolved from Structured Programming to Structured Analysis for Embedded Real Time Systems over the last 15 years. ProMod currently supports DeMarco's "Structured Analysis" for data-flow oriented requirements analyis, augmented by Hatley's and Pirbhai's approach to model dynamic system behaviour using state transition models and rules to integrate these models in the traditional data flow models. For the architectural (or system) design ProMod supports "Modular Design", based on D. Parnas'principles of information hiding and abstract data types. The methods also integrates the traditional Structured Design approach (Constantine, Myers, Page-Jones). Detailed design is supported using Pseudocode and stepwise refinement, which naturally lead to Structured Programming, independent of the chosen programming language.

In ProMod, these methodologies are supported by an integrated set of tools, working from a common software engineering database and within a uniform user interface. For each methodology interactive, graphic editors and text editors are provided, to allow the analyst and the designer to construct the models according to the rules of the methods. While editing a number of syntactical and semantical checks are provided to guide the developer and provide error-feedback as soon as possible. To check the consistency of whole models (or larger parts of it) the environment provides analyzers for each development phase. These analyzers maily detect inconsistencies between various objects (or views) in the models and they report missing or incomplete portions of the models. A flexible report generator allows to produce documents of all the models, including various generated cross reference lists, hierarchical structures, etc.

To bridge the gap between the different steps in the development cycle the environment also comprises transformers. One transformer takes the completed requirements specification and transforms it into a first suggestion for a hierarchical architecture design, which is then used to be completed with the design tools. The design information can automatically be transformed into code frames for various languages like Ada, C or Pascal to provide a starting point for the programmer.

In order to make ProMod acceptable in a wide variety of applications and companies it is supported under two different operating systems, i.e. VMS on VAX-machines and MS-DOS on PCs.

Experiences about using the methods and the tools are presented from a variety of application areas, showing how the methods and the tools influenced the quality and the productivity in projects during the last five years.

Database Support for Software Engineering Environments

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Advanced integrated design systems like software engineering environments rely on large quantities of highly complex and strongly interrelated information. Obviously, true integration in such systems requires sophisticated means for information management. Database concepts like problem-oriented data modeling, consistency control, recovery, data independence etc. are thus desirable and, ultimately, indispensible features for their efficient construction and operation.

Unfortunately, currently available database products are far from optimal for these specific applications. The reason is that they have been built with traditional business/administration type of applications in mind and thus lack the capability to deal with complexly structured data in an efficient way.

We report about the DAMOKLES project where a new database system is being designed and implemented that aims at overcoming the experienced difficulties. Its salient features include the following:

- The DAMOKLES data model (called DODM for Design Object Data Model) is based on composite objects. Besides the traditional attributes, they may contain subobjects that are objects in their own right. Thus, arbitrary object hierarchies as well as general object structures (by virtue of objects that are subordinate to more than one other object) can be defined. All objects are uniquely identified by surrogates.

- Objects may have versions that account for the representation of the temporal or alternative development of design information. A specific set of operations (beyond those for objects in general) is provided to exploit the semantics of versions.

- Objects as well as individual versions of objects may be related in arbitrary ways by applying the concept of n-place relationship. Again, all appropriate operators to retrieve and manipulate information based on relationships it undergoes are provided.

- A special attribute type "long field" is offered to capture large chunks of unstructured information. Thus, the facilities of conventional files are available under the auspices of the database system.

- DAMOKLES supports multiple logical databases that may be distributes accross a number of professional workstations and servers. For example, private databases for the individual engineer, team and project databases as well as public library databases may be defined and maintained.

- Besides the classical concept of (short) transaction, long-term units of work (sometimes - slightly incorrectly - termed "long transactions") are supported based on a mechanism to check out objects from a database and to check them in again after completion of the desired activities.

- Object-based mechanisms for access control allow for the selective authorization of user roles for retrieval and manipulation of information.

- A basic mechanism for the enforcement of complex consistency constraints is also included.

A prototype of DAMOKLES (which currently demonstrates the data model only) is operational and used in the UNIBASE software engineering environment currently built in the context of a major German cooperation project between 8 software houses and research institutions. Our present work is geared towards the distribution of databases, and the remaining features are planned to be incorporated by 1989.

Sigma(Software Industrialized Generator and Maintenance Aids) system and Workstations

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Sigma system aims at a better software development environment for improving software quality and development productivity. The concept of the system is to make development environment independent of various target computer systems. And for the development system, it is designed as a distributed development environment based on powerful personal workstaions and tools on them which are connected to LAN and/or WAN.

Sigma Operating System

For the independent development environment, a common OS interface has been considered and defined. The OS will have necessary and sufficient functions for software development and will give common interface to many precious good tools for better portability. This will enable users of the Sigma system select favorite tools regardless of the difference of workstations or favorite workstations regardless of the available tools on them.

Sigma operating system interface is based on UNIX operating system developed and licensed by AT&T. Some functional additions were made to UNIX so as to match the Japanese environments and for better portability of the tools running on the OS. The UNIX part is mainly from System V and some from Berkeley version particularly communication functions. Other enhancements done to the interface are Japanese language processing capability, multi-window, graphics and relational DBMS interfaces. Further enhancements are being considered, and the trends of standardization, either formal or de facto are carefully observed.

The implementation of the OS is left to each company who wishes to commercialize it.

Workstations

One of the key factors of Sigma system is workstations. The basic standpoint of the system is not to specify any hardware specification. Any hardware on which the OS can be regarded as Sigma system hardware.

Achieving the objectives of the system, however, each personnel involved in the software development are assumed to have the powerful and sufficient computing power, in other words, these

personnels are expected to have their own workstations, and they can use workstations whenever they need or want without any restrictions. Hence at the early period of the system planning, not specifications but a brieff guideline of the workstations were announced. It described as follows:
32bit microprocessor with 1 MIPS processing capability, 4 Megabyte main memory, 80 Megabyte hard disk, 1,000 × 1,000 bitmap display with mouse-type pointing device, and a few communication interfaces, etc. There was one important point in this guideline. That was the price. For the sole personal use of the workstation, it would be desired between 1,000,000 Yen to 2,000,000 Yen by 1990 when the system will be widely used. (1DM is approximately 80 Yen as of August 1, 1987)

Table 1. Hardware Requirements of Prototype Sigma Workstation

【Control mechanism】	
CPU	32-bit internal register
Floating point	A floating point calculation mechanism is necessary, internal expression is IEEE format
Main memory	4 MB (minimum)
Logical area	8 MB (minimum)
【File mechanism】	
Hard disk	Minimum user are 20 MB
Floppy disk	5"(2HD) and 8" (2D) for data transfer
Back up	System must have back-up function
【Display mechanism】	
CRT resolution	Graphic display: 1024 x 768 dots or more Text display (Kanji: 24 x 24 dots) 40 characters x 24 lines
Keyboard	Key layout is JIS standard 10 function keys (minimum)
Mouse	Two or more bottons
Printer interface	Not specified for prototype
【Epxternal interface】	
Serial interface	Two RS232C (V. 24) (minimum)
Parallel interface	Centronics interface (option)
LAN interface	IEEE 802.3 standard
Interface for DDX-P	V. 28 (X. 21 bis) or V.11 (x.21)
GPIB interface	ICE interface (option)
【Copy prevention mechanism】	(Hardware protection mechanism considered)

Later, the technical and industrial feasibility were discussed

and detailed requirements were announced in July, 1986. The requirements define some of the hardware features which may affect the software portability.

The gist of the requirements are shown in table 1. The price of 3 million Yen for shorter target (by the end of the year 1987) was also indicated.

Prototype Sigma workstation are now available from some hardware manufacturers. At present, approximately 200 of them are supplied to Sigma project and being used to test and integrate Sigma OS and also usd to develop programs such as tools for Sigma users. Suppliers of these workstations are counted up to 10 manufacturers. Some of these prototype workstations have hardware configurations derived from the existing engineering workstations. They cover all the Sigma hardware requirements except the price. Although the requirements do not mention the physical size and installation conditions of the workstations, the market requires more compact machines for Sigma usage.

All these 10 manufacturers are preparing to announce new products which satisfy the both Sigma and market requirements. In fact, a few companies have already announced and released the new Sigma workstations.

Differentiation will be done in price, size, performance and the total usability including maintenance. Sigma expects these differentiation for future improvement and dissemination of the system.

The future

The Sigma project started in mid 1985 and now it is two years old. The prototype of the system will be available soon for experimental use by monitors. The workstations will also gradually be purchased by the monitors and tested fully in the commercialized market. Even today, almost all the workstations surpass the Sigma requirements, particularly speed and memory size both main and auxiliary. This will continue as software require more and more speed and memory for faster response with better man-machine interface. It is expected that hardware technology makes this possible. As for Sigma, there should be two tasks remained to workstations:

(1)To mature the whole software development environment provided by Sigma using powerful component, i.e. workstations.

(2)Towards the real Sigma system in full use from 1990, to define further necessary interface to software to assure better portability, as well as to show a newer up-to-date guideline for progressed component in the improved environment.

Overview of Sigma Multi-Media Window System(Sigma MMW)

N. Akima

Information-technology Promotion Agency, Japan

1. Multi-Media Window System

Of the tools which Sigma project has scheduled for development, there are tools which handle text and graphics at the same time such as documentation support tools, requirement definition tools, and design tools. There are those who wish to use images as graphic data and to embed tables and graphs in text as graphic data.

The multi-media window system supplies several virtual devices (terminals) which allow mixed display and printing of multi-media (text, graphics, images). Input/output to the screens is through the creation of a virtual terminal. A portion of this virtual terminal is displayed on the screen as a window. Printing by tools is made in the same manner as display except that the virtual terminal only handles output. The paper size is designated by creation of a window.

The multi-media window system is a comprehensive system which includes display to the screen, mouse and keyboard input, operator interfaces, printing, menus, and icons. The concept of the multi-media windows is shown in Figure 1. Considerations will continue to allow to handle all forms of data including audio and animation in the future.

2. Multi-Media Window Design Policy

(1) To supply a uniform multi-media window interface for tools.

(2) To realize an interface independent of powerful hardware in order to increase portability of tools.

(3) To determine external conditions of the operator interface in order to make the basic functions of the man-machine interface the same, even among different computers.

(4) To establish an application interface for printintg equivalent to the display system based on the concept of WYSIWYG (What You See Is What You Get).

3. Display

The window system will transfer the display data of the various virtual terminals to the display screen of the actual terminal device with no interference between the data. Also, the window system will allocate the input data from the input devices (keyboard, mouse) to the buffers of each device of virtual terminal.

The virtual terminal which displays multi-media consists of a virtual plane, logical screen, and scope.

The tools define as many logical screens as necessary corresponding to the various types of data (media) and output the data to be displayed on these logical screens. Also, tools allow a number of logical screens to be positioned as desired within the virtual plane (display screen of virtual terminal). At this time, the logical screens can be ositioned so that they overlap each other. Moreover, a rectangular area called a "scope" can be set within the

virtual plane, and the window system will transfer the contents of this scope to the corresponding rectangular area on the physical screen. As a result, multi-media data can be mixed and displayed within a single window.

4. Printing

The basic concept is the same as the display system except that a printer is substituted for the virtual terminal. The same control commands as the display system are used.

Virtual devices for printing multi-media are comprised of a virtual plane and logical screens. There is no concept of the scope found in the display system. Setting the virtual plane determines the printing area. In other words, the size of the paper is set. The tools define as many logical screens as necessary corresponding to each media and outputs the data to be printed on these logical screens. Also, tools allow a number of logical screens to be positioned as desired within the virtual plane, in the same manner as display. At this time, the logical screens can be positioned so that they overlap each other. The main differences between the display system and printing system are outlined below.

(1) When data is output, it cannot be seen until printed. Printing instructions are made from the tools by commands.

(2) Any cursor control commands designated for text logical screens will be ignored.

5. Implementation

Various methods are possible for realizing multi-media window system. In order to realize the system as quickly as possible, an existing window system is taken as the base, and an interface conforming to the multi-media window system in that system is constructed. The following systems were considered as possible candidates for realizing the multi-media window system.

(1) X-Window

(2) GMW

(3) NeWS

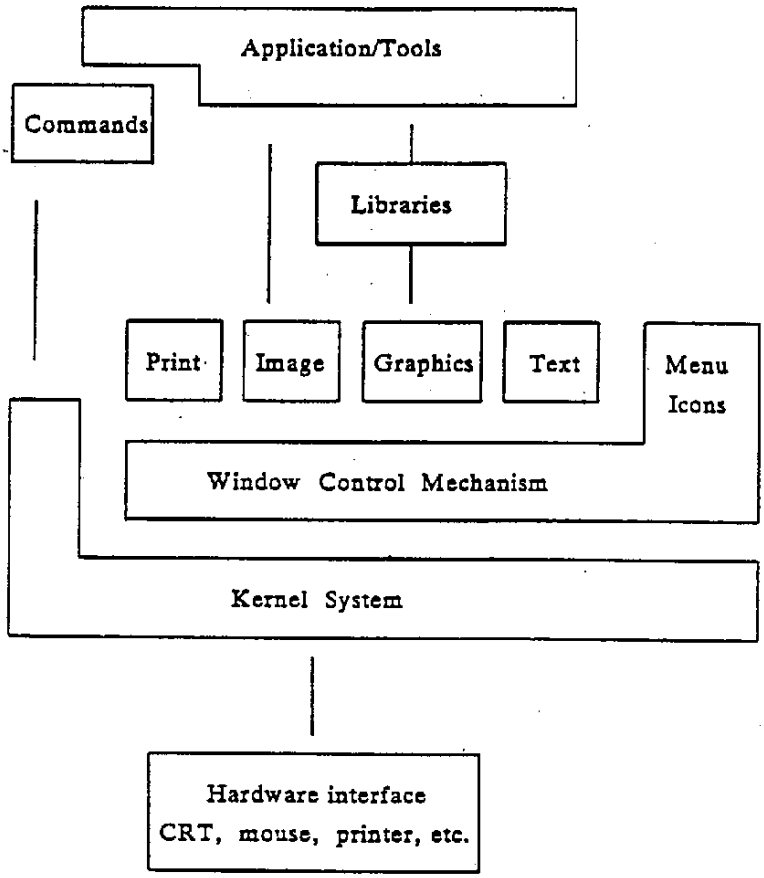

Figure 1 Overview of Multi-Media Window Function

The Joint Venture Project

"EUREKA Software Factory"

H. Abbenhardt

Softlab GmbH Munich

EUREKA is the name of the European high-tech research programm which has been set up in 1985. The EUREKA Software Factory (ESF) is one of about 170 projects in the EUREKA framework.

The primary objective of the ESF is a considerable advancement of industrial development of software. The basic idea that is persued here is to substantially improve the reusability of software. In order to achieve this, new software engineering methods and very powerful software tools are required.

The expected benefits are the considerable lower resource investments (manpower, time, direct costs), the improved reliablity and the higher quality of the developed software systems. The necessary know how and the occurring costs cannot be met by individual companies or even national consortiums alone. The European team work within the scope of EUREKA therefore offers a suitable frame for this project.

The concept of the project is based on a precise analysis of the initial situation with respect to the development of tools, tool boxes and software development environments. The analysis is also based on the experience that the partners of this project have gained in similiar projects and with products in the software engineering field.

ESF is a highly integrated, open and flexible environment for the production of complex modern software systems. It is the objective of this project to implement ESF so that it can be adapted to a great number of very different project and organisation types. By using a reconfigurable and modular structure it is possible to achieve this broad application spectrum.

At the moment there are 14 members in the ESF consortium coming from 6 European countries.

The ESF project is split into two phases:

- the Definition Phase (approx. 1 year)
- the Main Phase (approx. 9 years)

The Definition Phase started in September 1986.

In order to carry out a project with the technical and organisational complexity of ESF, thorough planning and coordination of tasks involved are absolutely necessary. It is the job of the Definiton Phase to prepare the basics for the whole ESF project. This is true for the technical frame, the project organisation and the legal basis of the project. The main technical results achieved in the definition phase are:

- a study of the requirements for software development environments considering the entire lifecycle, different project sizes and various application areas
- the definition of the ESF requirements
- the first design of the ESF architecture.

7．半導体分科会アブストラクト

7. 半導体分科会アブストラクト

"Two-Dimensional Electron Systems in Compound Semiconductors"

M.H. Pilkuhn, Stuttgart University

Abstract

Potential wells of very small dimension leed to quantized states for charge carriers. In the case of ultra thin layers in heterostructures of compound semiconductors, two-dimensional electron systems have been achieved and studied extensively with the respect to fundamental properties and applications. Of special interest are the advantages of two-dimensional systems for high speed transistors and semiconductor lasers.

The technology for fabricating quantum well structures with compound semiconductors will be described, especially the epitaxy with metallo-organic compounds in the case of the system InGaAs/InP. The properties of semiconductor lasers will be discussed in detail for the two-dimensional systems GaAs/GaAlAs, InGaAs/InP and GaSb/AlSb. This includes the discussion of recombination mechanisms in two-dimensional systems as well as the quantization of higher lying energy bands.

At high carrier densities, two-dimensional electron whole plasmas can form in small size heterostructures. The properties of these high density to deep plasmas are described. Strong many body effects leading to a band gap pre-normalization are observed and a review of recent results will be given.

AlGaAs/GaAs Quantum Well Laser for OEIC Application

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1. Introduction

Semiconductor lasers with quantum well(QW) active layer show superior characteristics of low threshold current oscillation, high characteristic temperature and high relaxation oscillation frequency compared to conventional double heterostructure(DH) lasers. They also have advantages for device designing; emission wavelength can be controlled by well width selection, and planar buried heterostructure can easily be formed using diffusion-induced disordering of the QWs. We have studied the QW lasers aiming at low threshold current operation with simple structure from the standpoint of application to OEIC transmitters. In this paper, AlGaAs/GaAs QW lasers applied to OEICs are reported. A new buried heterostructure(BH) multi-quantum well(MQW) with simple and planar structure is also described.

2. Epitaxial growth of quantum well structure

Defect-free and highly uniform epitaxial multi-layers with steep hetero-interface are required for high performance QW lasers. Molecular beam epitaxy(MBE) is a promising growth technology to fulfill such requirements, especially to realize a steep hetero-interface. In growing high quality AlGaAs/GaAs crystals by MBE, both careful outgas treatment and growth at slightly high temperature around 700℃ are essential. Crystal

qualities of MBE grown QW layers heve been studied by photoluminescence(PL) measurement. Figure 1 shows the photon energy at peak luminescence intensity from the AlGaAs/GaAs single quantum well(SQW) layer as a function of well width. Observed peak energy agrees well with the calculated value of n=1 electron-to-heavy hole transition, which suggests the formation of good QWs. Measurements on spatial distribution of PL intensity and peak energy for the SQW over the wafer indicate high uniformity in crystal quality as well as alloy composition of the grown layers. The PL intensity of QWs has been improved further by introducing a superlattice buffer(SLB) layer.

3. Laser characteristics

Three kinds of QW lasers with ridge waveguide stripe geometry have been fabricated. These QWs are MQW, graded index waveguide and seperate confinement heterostructure(GRIN-SCH) SQW, and GRIN-SCH SQW with SLB. The representative threshold current dependences on the laser cavity length are plotted in Fig.2. Data for the conventional DH lasers with the same ridge waveguide are also shown. Drastic reduction of threshold current is realized with the QW lasers. The GRIN-SCH SQW lasers with SLB show the lowest threshold current among them reflecting high quality of the QWs, and a threshold current as low as 5 mA is attained with cavity length below 330 μm. The threshold current density estimated for this laser is as low as 175 A/cm^2. Further reduction of threshold current to a few mA has been achieved by increasing facet reflectivity. A differential quantum efficiency as high as 80%, a power over 30 mW/facet, and almost single longitudinal mode oscillation are attained in the GRIN-SCH SQW laser with SLB. The characteristic temperatures measured in the temperature range between 0 and

80°C are 160K for the GRIN-SCH SQW laser and 205K for the MQW laser. As for the reliability of the QW lasers, very high carrier and photon density are anticipated in the QW region. Figure 3 is the result of aging test of eleven GRIN-SCH SQW lasers with mirror coated. The value of current degradation rate between 200 and 4000 hours over all the lasers tested is as small as 2%/kh, suggesting a high stability of these lasers. A LD/DRIV/MON OEIC has been fabricated incorpolating such QW lasers, and high bit-rate operation over 1 Gb/s has successfully been attained.

4. Lateral current injection MQW laser

We have fabricated an MQW laser with a new planar BH by using diffusion-induced disordering as shown in Fig.4. In this structure, a planar BH for index guiding is easily formed and homogeneous current injection to each well is possible due to lateral injection scheme, which leads to a high degree of freedom in designing the MQW structure and is also suitable for OEIC application. The lateral current injection (LCI) MQW laser shows an extremely low capacitance because the facing area of impurity diffused electrode regions is very small. A chip capacitance of 0.27 pF has been attained. This value is, at least two orders of magnitude lower than that for conventional lasers. This structure is therefore promising for ultra high speed laser and OEIC application.

5. Summary

AlGaAs/GaAs QW lasers with simple ridge waveguide has been fabricated using MBE. The GRIN-SCH SQW laser with SLB shows very low threshold current less than 5 mA. The LCI MQW laser with a new planar BH has also been demonstrated.

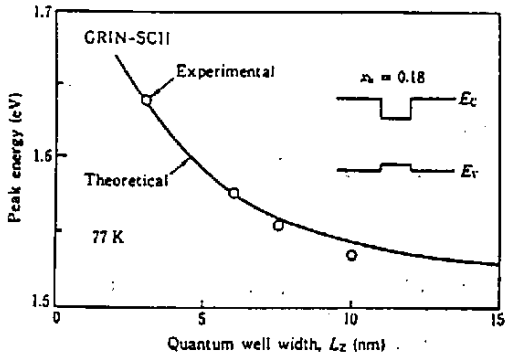

Fig. 1 PL peak energy as a function of well width for AlGaAs/GaAs SQW.

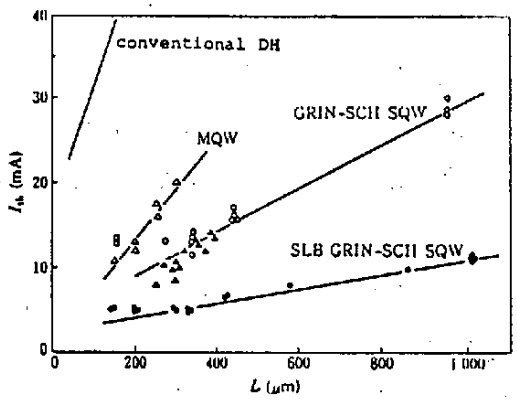

Fig. 2 Cavity length dependence of threshold current of ridge waveguide DH, MQW, GRIN-SCH SQW, SLB GRIN-SCH SQW laser.

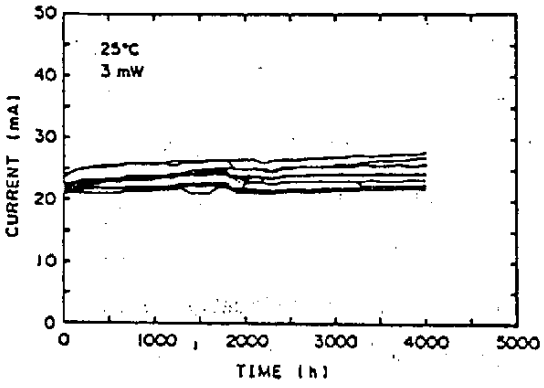

Fig. 3 Operating current variation for GRIN-SCH SQW lasers.

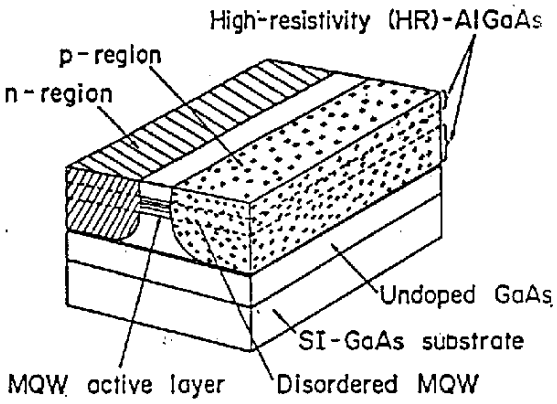

Fig. 4 Schematic structure of LCI MQW laser.

CHARACTERIZATION OF SEMICONDUCTOR CRYSTALS USING SYNCHROTRON RADIATION

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Synchrotron radiation (SR) is one of the most promising x-ray sources to realize a quick and informative x-ray measurement, because of its high intensity, collimation, continuous spectrum, time pulsation and polarization states. The x-ray optics for diffractometry or topography with SR consist of the geometrical crystal arrangement in a manner substantially similar to laboratory x-ray works. The big difference of the SR from the ordinal x-ray source is a selectivity of the wavelength with a sufficient intensity. Therefore, one can obtain x-ray data emphasizing an absorption edge of a peculiar element of the sample (a typical example is EXAFS measurement).

An advantage of using the SR is well demonstrated when a monochromator and a collimator are successfully set to deliver an extremely collimated, monochromatized x-ray beam with a small energy bandpass. In our case, 6 inch diameter, 1 cm thick dislocation-free silicon crystal disks are used as a monochromater and a collimator, each of them being placed on a water-cooled stage of a high-accuracy goniometer for the synchrotron beam from the 2.5 GeV storage ring at Photon Factory in National Laboratory for High Energy Physics (in Tsukuba).

Our present aspects of applying the SR to the semiconductor

crystals are as follows; (i) plane wave x-ray topography sensitive to a very small strain (lattice tilt and/or lattice parameter variation) in semiconductor bulk crystals or epilayers, (ii) x-ray diffractometry with an extremely small incidence angle of x-ray (grazing incidence x-ray diffraction) to study a two-dimensionally reconstructed super-structure at a semiconductor interface, (iii) diffuse scattering experiments for the study of local atomic arrangement in distorted alloys and other materials, (iv) fluorescence x-ray analyses of impurities on the semiconductor surfaces, (v) EXAFS studies of ternary or quarternary crystals, and (vi) others.

It is often needed to investigate a crystalline structure or strain in a thin epilayer (including a supperlattice), or perfectness of a bulk crystal such as a large diameter Czochralski-grown (CZ) Si wafer for VLSI or a liquid encapsulated Czochralski-grown (LEC) GaAs wafer for high speed devices. Employing an assymmetric reflection to make the incident x-rays very parallel (i.e., plane wave x-rays), we can investigate a lattice strain in a CZ Si wafer as small as 10^{-6} probably due to a concentration variation of unintentionally incorporated oxygen, as seen in Fig. 1, and can obtain an equi-Bragg-condition contour map for a LEC GaAs wafer, as seen in Fig. 2(a), relating to the dislocation distribution formed during the growth (its transmission topograph is shown in Fig. 2(b)).

Using the same equipment as the plane wave topography except an arrangement of the third goniometer, we can carry out the grazing incidence x-ray diffraction study to detect a two-dimensionally reconstructed super-structure at an interface such as a-Si/$Ge_{0.2}Si_{0.8}$(111) or Al/GaAs(001). The rotation axis of the third

goniometer is nearly vertical, while those of the monochromator and the collimator are horizontal for the SR. Thus, the x-ray beam was impinged on the sample under the condition of 0.2° grazing incidence angle, as schematically shown in Fig. 3(a). It was found that, even after the deposition of a thin a-Si film on a (5x5)-reconstructed $Ge_{0.2}Si_{0.8}$ surface, the Bragg reflections are still observed around some of the (m/5,n/5) fractional reciprocal lattice points, as shown in Fig. 3(b). This means that there remains a super-structure at the interface. Similarly, a (4x6)-reconstructed super-structure exists at the Al/GaAs(001) interface, which is much interested in terms of the Schottky barrier height formation mechanism.

Although other experiments are not described here, semiconductor material characterization using the SR are full of promise. Especially, time-resolved in-situ observation of rapidly proceeding phenomena in combination with more intense synchrotron sources would give a number of clearer understandings in semiconductor materials science.

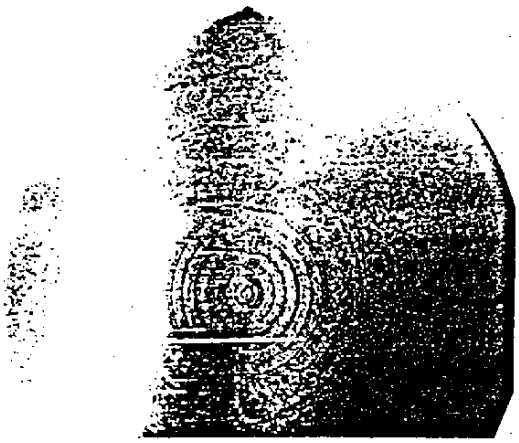

Fig. 1. Plane wave x-ray topograph of a 6 inch CZ Si obtained by using an extremely assymmetric reflection (under the total reflection condition).

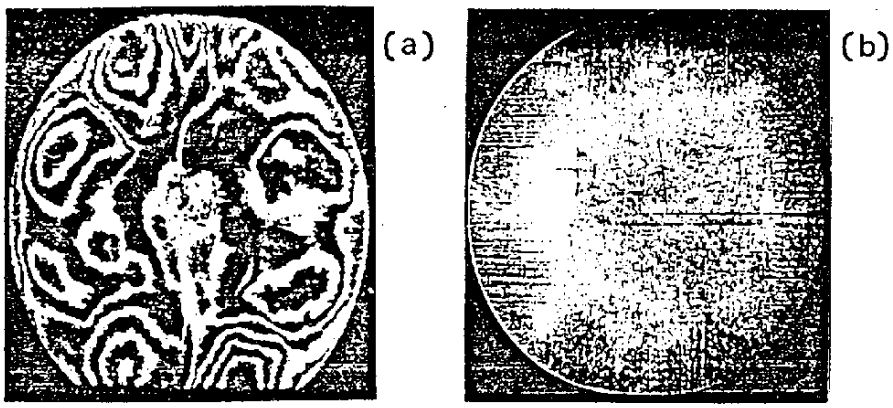

Fig. 2 (a) Superimposed pattern of a series of plane wave x-ray topographs of a (001) LEC GaAs taken around a Bragg peak at intervals of 10 seconds of arc, and (b) usual anomalous transmission topograph showing a high dislocation density at eight portions near the periphery.

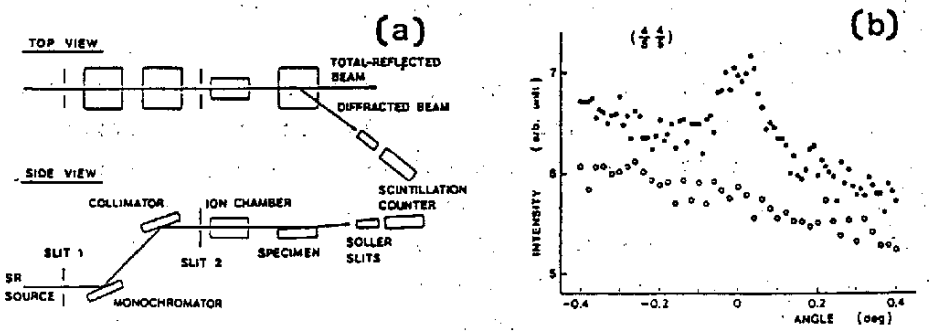

Fig. 3. (a) Scheme of grazing incidence x-ray diffraction, and (b) diffraction profile from the interfacial reconstructed super-structure of a-$Si/Ge_{0.2}Si_{0.8}$. The profile indicated by open circles is for a reference sample having no (5x5)-reconstructed surface.

High Resolution Optical Analysis of Defects in Semiconductors

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The production of semiconductor devices usually involves a number of processing steps in which the semiconductor samples are subjected to heat treatments, implantations and plasma-assisted etching procedures. Several different microscopic defects are produced unintentionally during these processes. The detection and characterization of the small, but for devices detrimental, amounts of defects is best accomplished by highly sensitive, non destructive, optical techniques. In this talk, characteristic examples will be presented of the optical investigation of process-induced defects.

During plasma-etching processes, ions from the plasma bombard onto the semiconductors surface with energies up to 2keV. Although the energies are much smaller compared with conventional ion implantation, similar defects are produced. We observe after plasma etching of silicon samples in different noble gases a family of defect centers involving the noble gas atoms. The large penetration depth of the noble gas atoms below the surface can only be explained by a diffusion mechanism enhanced by the damage created at the surface. A hydrogen plasma is commonly used to passivate undesirable defects in semiconductors. However, atomic hydrogen also neutralizes shallow donors and acceptors, thus increasing the electrical resistivity of the wafers. We have detected the interaction of hydrogen with impurities in the photoluminescence spectra. The comparison of the passivation in different semiconductors leads to a simple model of a hydrogen-impurity complex.

Analysis of Oxygen in Silicon

During the growth of Silicon crystals from the melt by the Czochralski (CZ) technique oxygen is incorporated into the crystal lattice. Due to the temperature-dependent solubility of oxygen in Si several agglomeration processes are observed during thermal processing of CZ-Si after crystallization. These phenomena are technologically important as well as scientifically challenging. If appropriately studied, some of them can be favorably used in the course of device manufacturing processes. Together, all these phenomena may serve as an example of the complex behaviour of an impurity in Si (other important partly electrically active impurities are for instance, C, N, or H). The possible modes of oxygen incorporated in Si range from O-atoms on interstitial lattice sites forming Si_2O-molecules to "clusters" of O-atoms. The smaller ones of such clusters (several O-atoms) usually are thought to be related to the so-called "thermal donors", whereas the larger "O-agglomerates" form separate oxidic phases within the Si-lattice as precipitates of different shapes (amorphous as well as crystalline). Interactions of O with other extrinsic and intrinsic defects are also known. These different O-related defects have been investigated with the standard techniques used for the characterization of defects in semiconductors by many researcher. Most of the different O-related defects can be studied in more or less detail especially with infrared absorption spectroscopy and important results were obtained by using this technique. Accordingly, the content of the talk will consist of a review of the different oxygen related defects in Si with emphasis on interstitial O and thermal donors.

WAFER DESIGN FOR SILICON DEVICE

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Concept of wafer design is now applied widely in Japan for VLSI, ULSI, ASIC and power devices and the first proposer are forgotten. This concept was proposed by me for the resume of Cooperate Laboratories of the VLSI Technology Research Association at the third meeting of Microelectronics Measurement and Technology Seminar held at San Jose[1]. After that, I blushed up the concept for Silicon wafer for VLSI device and I wrought two papers[2,3]. Recently, I introduce this concept into the wafer for power devices[4].

This concept was started from the talk of a salesman in 1972. He said that "A" Silicon device manufacturing facility got high yield using certain specifications "X", but "B" Silicon device manufacturing facility didn't accept the specification "X" for the reason of low yield. And specification "Y" Silicon wafers accepted by "B" facility for the reason of high yield, but the specification "Y" didn't accepted "A" facility. Firstly, I could not believe the talk. Then, I pursued the story and investigated widely. The results showed that the sales man was not storyteller. The correlation between die-sorter yield for each device, specification and vendors are shown following table:

Si device	facilities	Vendor U				Vendor V	
		High Coi		Medium Coi		Medium Coi	High Coi
		p-type	n-type	p-type	n-type	p-type	n-type
N-MOS	A	Low		High		Low	
	B					High	
C-MOS	A		High		Low		Low
	B						High

This relation are keep in recently as same as 15 years ago.

In 1973, Mr.Yasuami and I studied the correlation between heat treatment and precipitation of oxygen in Si wafer using X-ray section topography technique[5]. This work was the first step of wafer design. The second step was established in VLSI cooperate Laboratories from the 1976 to 1980. During the research works at VLSI Cooperate Laboratories, I could get the chance gathering the many fundamental knowledge for the wafer design.

The basic concept of wafer design is founded on the correlation between the thermal profiles of device process, oxygen behavior in Si crystals, wafer outer dimensions and its stability for using exposure instruments and device structure requirement of physical and electrical properties. The main problem in this concept is the thermal behavior of oxygen. The basic oxygen behavior is explained by the thermal dependency of oxygen saturation concentration and its diffusion length in Silicon. Figure 1a shows the temperature dependency of oxygen saturation. For each saturation, the rate of nucreation and growth give different value shown in Figure 1b. In the device process, silicon wafers get many heat cycle 400-1200°C depending on

the purpose. Then, the differences of thermal profiles in each device process give different oxygen nucleation and precipitation in its number and its size distributions.

And, real Silicon crystals are get different thermal histories from crystal growth to device process in growing furnace and after heat treatment including oxygen donner annihilation. Figure 2 shows a results of simulation experiments for nuclei formation effect in crystal grower. This figure shows that there is very big change at 800°C in quenching temperature and 3°/min. in cooling rate. This critical temperature overlapped on real pulling machine condition.

Figure 3 shows a typical temperature profiles for C-MNOS and N-MOS devices and the right side in figure shows the oxygen thermal behavior. If device maker wont highest yield, wafer vendor should be select suitable CZ-puller including hot zone structure and its arrangements, its operating conditions and after heat treatment. By SEMI report, the yield difference between JAPAN and USA is 10-20% for 256K DRAM. This difference is not only oxygen precipitation but also surface treatment and flatness. The surface treatment and flatness problems also depends on user's requirements, that is his process requirement-cleaning process, using stepper, and others. For the power device, the situation is same. Recently, we have developed MCZ-NTD large diameter wafers for high power device usage in this point of view.

Wafer design is not so much so-called materials design as a textile design in apparel industry. In apparel industry, textile is designed and chosen according to purpose and its difficulty of processing. Wafer should be designed and chosen according to device parameter, structure and its fabrication processes.

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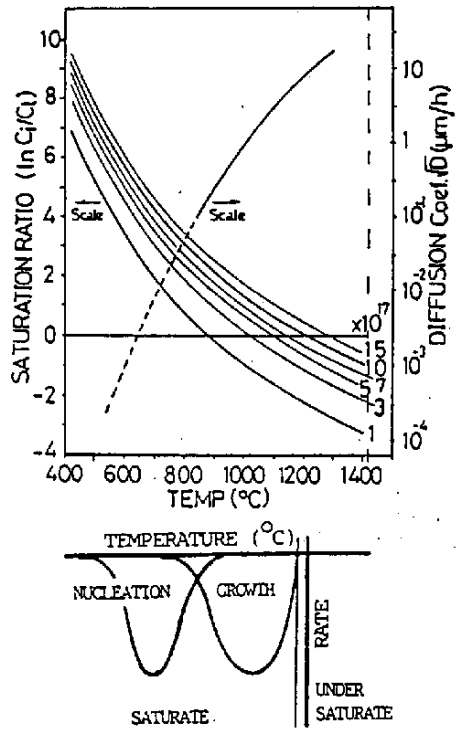

Figure 1 Saturation of oxygen in Silicon crystals a) and Thermal behavior of Oxygen precipitation.

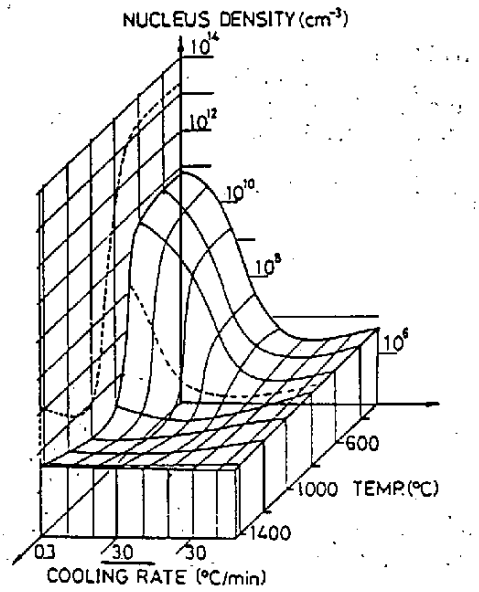

Figure 2 Experimental simulation of Thermal hysteresis in Crystal puller.

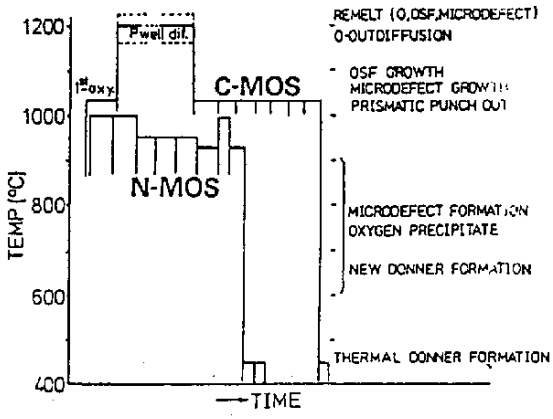

Figure 3 Schematic thermal sequence differences between N-MOS and C-MOS processes with oxygen behavior.

Abstract

High Resolution Electron Microscopy of Microelectronic Devices

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High-Resolution Electron Microscopy (HREM) of Si and GaAs microelectronic devices has matured into a valuable tool routinely used in the Siemens Research Labs. Applications of HREM to the characterization of Si-SiO_2, Si-a-Si, and III-V heteroepitaxial interfaces will be presented. The interpretation of HREM-images is often difficult; not only because of "optical" artifacts but also because the conceptual framework of defects in interfaces and their appearance on HREM-images is not too well understood. HREM-images of Si-silicide interfaces will be used to clarify some points in question.

High Resolution Observation of Fine Structure in Compound Semiconductors Using TEM, SEM, μ-RHEED and STM

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Recently, compound semiconductor devices have composed of very fine structures due to the progress of thin film formation and microfabrication techniques. The characteristic of the device is considerably influenced by the compositional abruptness in the heterointerface, the shape of multilayer structure, the crystal perfection, and so on. Thus, it is necessary to analyze these fine structures on the atomic order. Usual evaluation methods, however, can not satisfactorily meet to such a requirement.

In this review, new analytical methods developed in our laboratory using TEM, SEM, μ-RHEED and STM are described. These methods are able to succesfully evaluate fine structures such as the cross-sectional structure of multilayer, the compositional distribution in the superstructure and the atomic arrangements in the surface and interface.

A cross-sectional TEM observation of multilayer yields much information, because the entire structure in the growth direction can be viewed simultaneously in an image. This method is also helpful to determine the atomic arrangements in the heterointerfaces by the lattice image. However, it is difficult to know the change of composition quantitatively from the TEM image.

Kakibayashi et al. have proposed a new method for evaluating the Al composition in a GaAs/$Al_xGa_{1-x}As$ superstructure from a TEM image.[1] They call this method CAT(Composition Analysis by Thickness -fringe) for short. In this method, a wedge-shaped specimen formed by cleavage is used. Typical CAT images of superstructures with

different compositional abruptness in the heterointerface are shown in Fig. 1. A composition analysis can be made by observing the fringe shifts along the growth direction. The special advantage of this method is a high spacial resolution of better than 0.5 nm. The abruptness at the heterointerface and the compositional distribution in the thin layer could be succesfully evaluated from the TEM image. The CAT method was applied to evaluate the growing conditions in a newly developed MOCVD reactor. Fig. 2(a) and (b) show CAT images of $Al_{0.3}Ga_{0.7}As$/GaAs superstructures, which are made with two different rotation speeds of the substrate holder. A periodic fluctuation of the equal thickness fringe is clearly observed in the $Al_{0.3}Ga_{0.7}As$ layers. Hence, it can be seen that the Al composition x oscillates sinusoidally in the growth direction as a result of inhomogeneous Al concentration in the reactor. However, the straight fringe in Fig. 2(c) proves that a uniform $Al_{0.3}Ga_{0.7}As$ layer is successfully grown in the improved reactor. The CAT method is very useful for high resolution observations of fine compositional fluctuations.

A field emission SEM(FE-SEM) is a powerful method to observe the surface topography with high resolution. Kuroda et al. have developed a so called "in-lens" FE-SEM and shown to be able to directly observe the atomic layer step in the height of 0.45 nm on the surface of W single crystal.[2] The FE-SEM also gives full play to it's ability in an observation at low accelerating voltage. Fig. 3 shows the cross-sectional image of WSi_x on poly-Si/SiO_2/Si base which is directly observed without any metal coating at 7kV. The crystal size and fine structures of grain boundaries can be evaluated with 3-dimension in detail. The lower voltage observation will be get more important to eliminate the electron irradiation damage to the specimen and to decrease the charge-up phenomenon to the non-conductive materials.

A microprobe RHEED(μ-RHEED) is especially useful for studying crystal growths on substrates with atomic layer depth resolution by

performing in situ observations. This has been applied to analyze MBE growth mechanism when RHEED intensity oscillations occur.[3] Topography changes of Si surface during Si MBE are shown in Fig. 4. The surface topography changes repeatedly with the period of RHEED intensity oscillation and the shape of atomic steps does not change during the growth. This provides first evidence that RHEED intensity oscillations occur as a result of layer-by-layer two-demensional nucleation growth. This method should be combined with STM to observe the precise surface structure simultaniously.

A STM is one of the most effective methods for evaluating a topography and atomic arrangements on surface in atomic scale.[4] Fig. 5 shows the almost completed 7X7 structure on Si(111) clean surface. The special advantages of this method are to be able to observe surface atoms in the real space and to detect the atomic position in the depth direction from the contrast of the atomic image. Moreover, the elemental and bonding state analysis can be made from the contrast.[5] In this method, the in situ observation will be get more important thechnique.

Each methods have some characteristics as shown in Table 1. These characteristics can be applied to the evaluation of various subjects in compound semiconductors. Thus, compound semiconductors should be characterized multilaterally by applying their performances.

References

1) H. Kakibayashi and F. Nagata: Jpn. J. Appl. Phys. 26 (1987) 770
2) K. Kuroda, S. Hosoki and T. Komoda: J. Electron Microsc. 34 (1985) 179
3) M. Ichikawa and T. Doi: Appl. Phys. Lett. 50 (1987) 1141
4) G. Binning, H. Rohrer, C. Gerber and E. Weibel: Phys. Rev. Lett. 50 (1983) 120
5) R. J. Hamers, R. M. Tromp and J. E. Demuth: Phys. Rev. Lett. 56 (1986) 1972

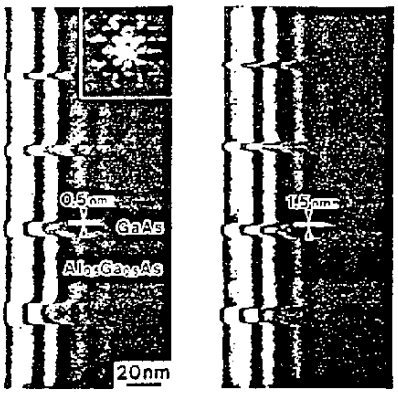

Fig. 1

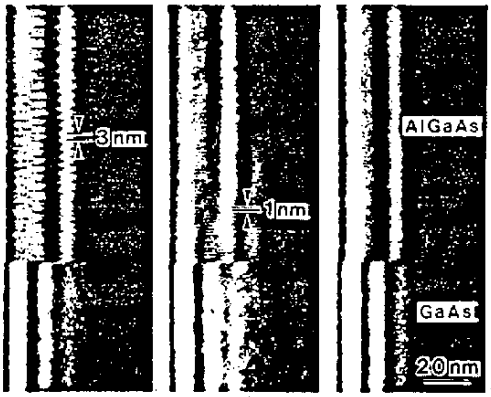

Fig. 2

Fig. 3

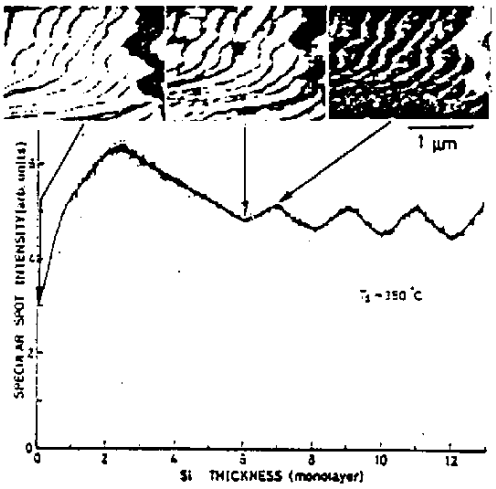

Fig. 4

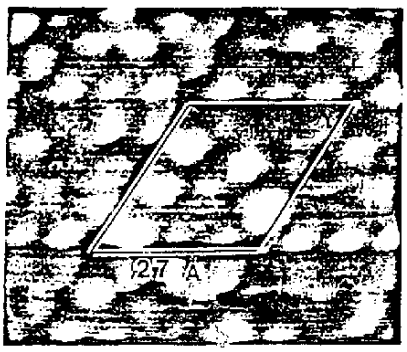

Fig. 5

Method	Characterization substances	resolution	Characteristics
CAT	compositional distribution in superstructure	0.5nm Al composition Δ±0.05	simultaneous observation of structure and composition in depth direction
FE-SEM	surface topography, microfabricated patterns	0.5nm	beam damage less, uncoating specimen
μ-RHEED	crystalline states and structure on surfaces	lateral 20nm depth 0.1nm	in situ study of surface reaction process
STM	topography and atomic arrangement on surface	lateral 0.2~0.3nm depth 0.05nm	direct observation of surface atoms in real space

Table 1

Electron spin resonance observation of defects in device oxides

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Electron spin resonance (ESR) experiments have previously identified two paramagnetic defects designated the E' and P_b which have subsequently been correlated with positive charge in the oxide and interface states respectively in thin SiO_2/Si. The experiments presented here observe these two defects and a third defect not previously reported in device oxides on silicon. In these experiments this defect, generally called the 74-G doublet when found in high-purity "wet" quartz, is found in quantities approxomately equal to the E' and, like the E', is distributed uniformly throughout the oxide. This result is substantially different than that observed in bulk quartz where previous reports generally see doublet quantities that are a few percent of the E'. The 74-G doublet has a g factor similar to the E' and thus presumably has a related electronic structure. However, unlike the E', it is hyperfine split by the presence of a nearby proton. It thus becomes the first major defect identified in SiO_2 on silicon at room temperature to involve hydrogen and thus the central issue surrounding the observation that hydrogen release at the SiO_2/Si interface is correlated with interface-state generation.

Following the original ESR report of the P_b and E' near the Si/SiO_2 interface by Nishi, first the P_b center and then the E'center have been intensively studied. First, Poindexter,

Caplan, and co-workers identified the P_b as a silicon atom with a dangling bond located at the Si/SiO_2 interface. After major contributions by a number of workers established the amphoteric nature of the P_b and identified it as the majority of the interface states, the emphasis has started to shift to include the E'. One reason for the interest in the E' is the search for the mechanism or mechanisms which produce interface states coupled with the recent ESR and capacitance-voltage (C-V) identification of the E' with a major part of the radiation-induced positive charge in the oxide. In particular, Winokur et al. and Hu and Johnson have argued that the formation of radiation-induced interface states is related to holes generated in the oxide and subsquently trapped near the interface. Griscom, making extensive use of the data on radiation damage effects in bulk SiO_2, has concluded that the experimental results on thin SiO_2 are consistent with the production and subsequent diffusion of radiolytic molecular hydrogen as the source of interface-state buildup. Although Hu and Johnson and Chang, Wu, and Lyon used only C-V to characterize their samples, these experiments are noteworthy because of the (1)introduction of vacuum soft x ray (VXR) as an efficient means of producing holes in the oxide without simultaneous drift to one of the interfaces and (2)demonstration that hole production is the first and reversible step in a multiple-step process leading ultimately to interface state formation.

Our presented here are not directly comparable to those of most device oxide radiation damage ESR experiments which have generally attempted to maximize P_b production by applying bias

during irradiation. However, it is possible that the observation of the doublet in the present experiments is due to either (1) improved signal to noise or (2) exceeding a damage threshold below which 74-G doublet production is not observed. Experimental and theoretical evidences combine to support the E' as positively charged and a major contributor of holes in radiation damaged oxide. The charge on the 74-G doublet is not known.

A significant body of evidence exists which suggests that the movement to the interface of some form of hydrogen is correlated with the buildup of interface states. Raidation damage is also correlated with the subsequent buildup of interface states. The observation of the 74-G doublet as both a major defect involving hydrogen and produced by radiation would seem to make this defect a potential intermediate for the formation of interface states.

Our experiments above suggest the 74-G doublet is a key intermediate in hydrogen assisted positive charge annealing of SiO_2 and must also be a good candidate for such a role in all processes correlated with the presence of hudrogen, namely, interface state formation and interface state annealing. Griscom, using an extensive set of published literature, has recently concluded that the buildup of interface states in SiO_2/Si is correlated with the diffusion of radiolytic molecular hydrogen and proposed a model based on this conclusion. In one reaction path of this model, E' somehow reacts with molecular hydrogen to release monatomic hydrogen which then reacts with Si-

H bonds at the interface to form interface states. But this is not quite correct or complete because the reaction of molecular hydrogen and E' forms 74-G doublet. However, making the single substitution of the doublet for monatomic hydrogen or a presursor of monatomic hydrogen in Griscom's argument, results in the same interface state formation mechanism but now with a very easily identified state immediately preceeding interface state formation.

The Physics of Gettering in Semiconductors

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TELEFUNKEN electronic, Heilbronn

The purpose of gettering is to prevent impurities from precipitating in electrically active regions of semiconductor devices and thus avoid enhanced leakage current and soft reverse current voltage-characteristics. The basis for handling gettering mechanisms is the understanding of the behavior of the respective impurities during technological processes. Although gettering has been applied for long times more systematic investigations started only recently. The first results will be reviewed in this paper.

Impurities which form precipitates especially in silicon crystals belong almost all to the group of transition metals. The most harmful metals are Fe, Cu, Ni, and Au. With the aid of solubility and diffusivity data the behavior of these metals during heat treatment of the crystal is discussed in order to explain their precipitation at the surfaces and in the volume of silicon wafers. An important role plays the nucleation of the impurities which depends on the crystal orientation and on the structure of the respective precipitate. First results of detailed TEM investigations on Cu-, Ni-, Co-, and Pd- precipitates in silicon will be presented. So far only crystalline silicides have been detected which fit more or less the silicon host lattice. These results agree well with recent haze investigations.

Besides the well-established methods to control the getter effectivity two new methods have been proposed recently: The palladium-test and the iron-test. These techniques based on haze investigation (Pd-test) and DLTS measurements (Fe-test) are briefly reported. As a first result it was found that iron (and in addition all lighter 3d transition metals) precipitates only via an heterogeneous nucleation process whereas Co, Ni, and Cu precipitate also via an homogeneous nucleation mechanism. Ni and Cu, however, prefer an heterogeneous nucleation and therefore they can be gettered in the same way as Fe impurities.

The basis of gettering is the intentional formation of nucleation sites. This can be performed by internal (intrinsic) or external gettering or by the generation of lattice defects due to a mechanical distortion of the wafer backside. Frequently unintentionally formed stacking faults act as the real nucleation sites. In order to obtain effective gettering several conditions must be accomplished which will be discussed in the paper.

Besides the intentionally formed getter centers there may be additional unintentional nucleation sites in the semiconductor material. Impurities which precipitate via an homogeneous nucleation process e.g. can act as nucleation sites for other metals. But even in pure starting material there are so far unknown defects which act as nucleation centers especially in the edge region of FZ silicon wafers and thus affect the homogeneity of wafers after processing.

With the aid of detailed knowledge about the behavior of transition metals in semiconductors and the new investigation methods it should be possible to improve traditional gettering methods and adjust the needed gettering efficiency to the respective impurity content in order to get best results which are required for VLSI application. Experimental data for the properties of transition metals in semiconductor crystals are available so far only for silicon. It is even still not known which impurities are important in GaAs and other III-V compounds. Since almost all III-V compound semiconductors exhibit more or less high densities of dislocations an effective gettering is not yet possible because the dislocations compete with intentionally generated nucleation sites.

Concept and Basic Technologies for 3-D IC Structures

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VLSI will be reaching to the limit of minimization in 1990's, and after that the further increase of packing density or functions might depend on the vertical integration technology.

3-D integration is expected to provide several advantages;
(1) Parallel processing (2) High speed operation
(3) High packing density (4) Multi-functional operation
High speed performance of 3-D IC is associated with shorter interconnection delay time, parallel processing and decrease of parasitic capacitance due to SOI structure. Capability of multi-function is one of the special features of 3-D IC. Each layer or a set of several layers can have their own functional performance. Also in device level, different performances, MOS and bipolar, and different characteristics caused by different process technologies can be assigned to each desired active layer. It will be possible to make use of these advantages for system design.

Basic technologies of 3-D IC are to fabricate SOI layers and to stack them monolithically. Crystallinity of the recrystallized layer in SOI has become better and better as shown in electron mobility improvement in Fig. 1. Very recently, crystal axis-controlled, defect-free single crystal area has been obtained in chip size level by laser recrystallization technology.(Fig. 2)

Some basic functional models showing the concept or image of a future 3-D IC were fabricated in 2 to 3 stacked active layers.

Figure 3 shows a SEM cross-sectional photograph and a schematic drawing of 3-level 3-D IC fabricated by using laser recrystallization of poly-Si. Each layer has its own interconnection and can be operated independently. Each active layer is electrically connected vertically through via-holes, and signals can be transferred between the layers.

Figure 4 shows a 256 bit static RAM fabricated in double active layers. Memory cells of 6 E/E type NMOS transistors were fabricated in the 1st layer, and a peripheral circuit such as sense amplifiers, I/O circuits and decorders in the 2nd layer.

Several types of image sensing devices integrated with primitive signal processing circuit in 3-D structure were also demonstrated.(Fig.5,6,7) A 10 bit linear image sensor composed of serial time driving of 10 elemental pair of photosensor and signal processing circuit with shift registers(Fig. 5) showed the signal output in serial timing(Fig. 6) with corresponding to the spatial illuminative photosignal to the linear sensor.

Some other proposals of sub-systems in the application of 3-D structure, and the technical issues for realizing practical 3-D IC,i.e., the technology for fabricating high quality SOI crystal on complicated surface topology, crosstalk of the signals between the stacked layers, total power consumption and cooling of the chip, will be discussed in this paper.

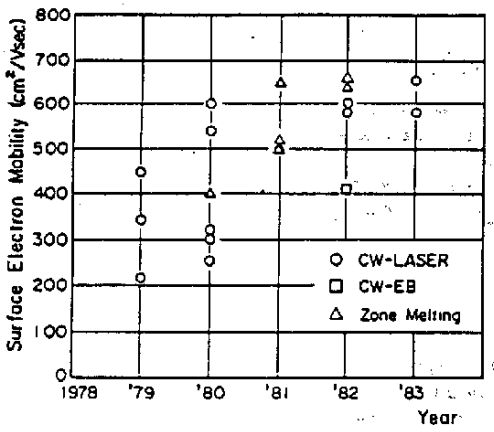


Fig. 1 Progress of surface electron mobility of MOS transistors fabricated in SOI layer. CW laser, Electron beam, Strip heater

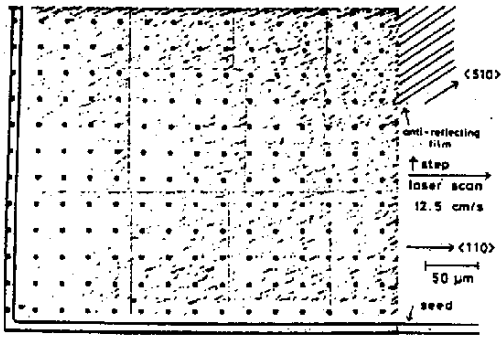


Fig.2 Photograph of a chip after laer recrystllization of poly-Si The crystal is almost completely axis-controlled and defect free.

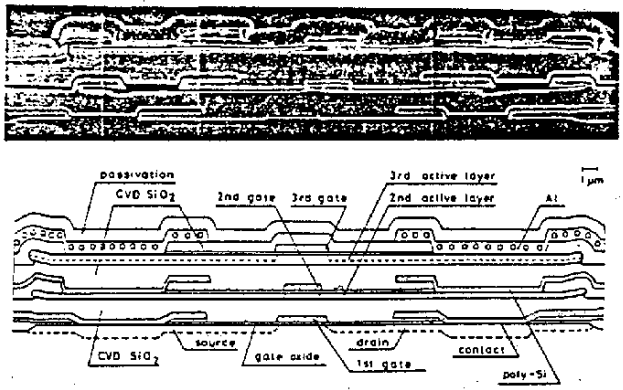
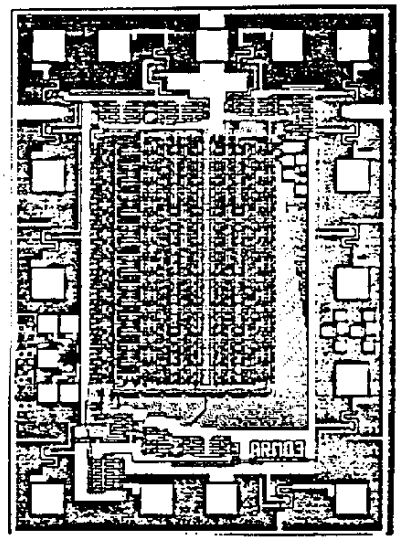


Fig.3 SEM cross-sectionmal photograph and a schematic drawing of planarized, tripply-stacked IC layers

Table 1 Feature and performance of a 256 bit static RAM fabricated in stacked structure.

Organization	256 X 1 bit full static RAM
Technology	3-D structure
	bottom layer NMOS
	top layer CMOS
Chip size	2.6 X 1.9 mm^2
Cell size	50 X 70 μm^2
Supply voltage	4 - 8 Volt
At supply voltage of 5 Volt	
Address access time	120 nsec
Active power dissipation	100 mW



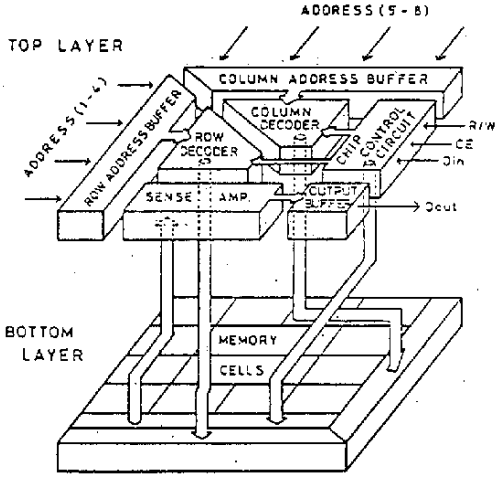


Fig.4 Chip photograph and a block diagram of stacked 256 bit static RAM fabricated in double active layers. Feature and performance of the RAM is shown in Table 1

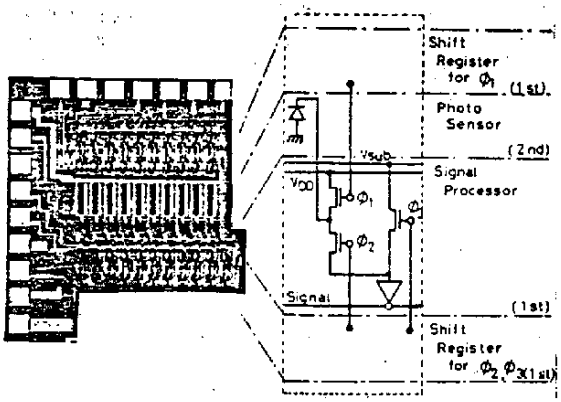


Fig.5 Photograph of a stacked 10 bit linear image sensor.

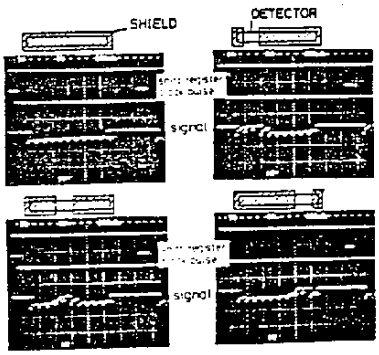


Fig.6 Examples of output signals of the 10 bit linear image sensor corresponding to the various photo input data pattern.

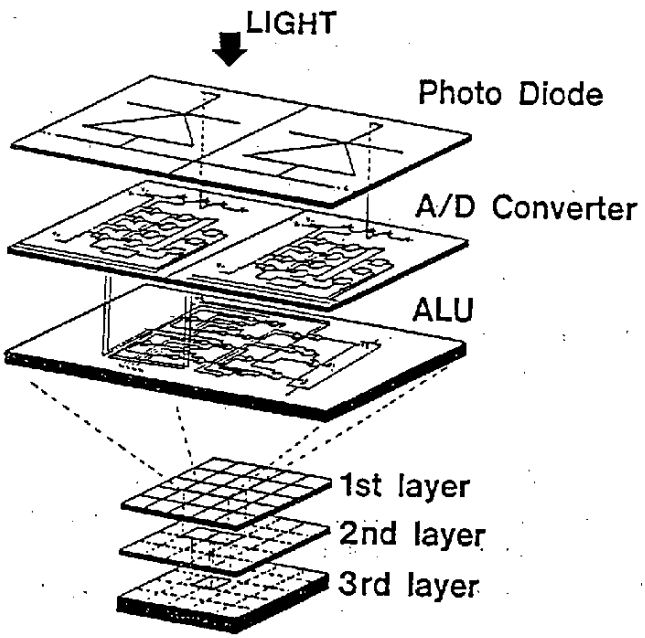


Fig. 7 A small-scale test device of one chip real time image processor fabricated in 3-layer 3-D IC.

Resist Technology for Submicron Lithography

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Progress in semiconductor manufacturing is normally exemplified by the shrink of critical dimensions in memory devices. The 1 Mbit DRAM with linewidths of about 1 µm is a reality today. The next generation, the 4 Mbit DRAM, requires 0.7 - 0.8 µm design rules.

Resist technology has to follow these requirements and offers a series of options to support the tendency to smaller geometries and better linewidth control. Dyed resists have been designed to reduce linewidth variations of resist lines over highly reflective topography. It can be demonstrated experimentally that light scattering is the dominant cause of severe distortions.

The image reversal technique is another means of increasing resolution by controlling the wall angle of the patterned resist. Application results of a unique new image reversal resist will be shown.

With the use of higher-numerical-aperture lenses topography on the wafer increases the depth-of-focus problem in optical lithography, so that multilayer processing may become obligatory. High resolution can be achieved with a newly developed three-layer resist system.

X-ray lithography undertakes high efforts to become a competitor of optical lithography. A three-component X-ray resist, using the principle of chemical amplification, is under development. Mechanistic aspects of the system will be addressed.

8. 第4回 日独情報技術フォーラム・プログラム

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SCHEDULE

OF THE

4TH GERMANY-JAPAN FORUM

ON INFORMATION TECHNOLOGY

I. Plenary Session

TUESDAY, OCTOBER 27TH 1987:

13.30 - 16.30	Sightseeing Tour Stuttgart by bus
13.30	Departure from Holiday Inn
13.45	Departure from hotel Schatten
15.40	Transfer from Holiday Inn to Meeting of all German participants by bus
16.00 - 17.00	Meeting of all German participants (Hotel Schatten)
16.50	Transfer from Holiday Inn to reception by bus
17.15	Transfer from hotel Schatten and Meeting to reception by bus
18.00	Reception by the Prime Minister of Baden-Württemberg, Dr. Späth (Neues Schloß, Marmorsaal)
approx. 19.40	Buses returning to hotels
20.30 - 21.30	Meeting of the Chairmen (Hotel Schatten)

WEDNESDAY, OCTOBER 28TH 1987:

8.35	Transfer from Holiday Inn to MPI by bus
8.50	Transfer from hotel Schatten to MPI by bus
	(1) Welcome Speech
9.30 - 9.40	Lord Mayor Rommel
	(2) Opening Speeches
9.40 - 9.50	H. E. Miyazawa, Ambassador of Japan
9.50 - 10.00	Dr. Ziller, Secretary of State
	(3) Opening Remarks
10.00 - 10.10	Prof.Dr. Engl and Prof.Dr. Yanai
10.10 - 10.20	Mr. Thomas, BMFT and Mr. Atarashi, MITI
10.20 - 10.45	--- Coffee break ---
	(4) Reports
10.45 - 11.30	Quantum Hall Effect (Prof.Dr. von Klitzing)
11.30 - 12.15	Higher Temperature Superconductors (Prof.Dr. Tanaka)
12.15 - 14.15	--- Luncheon ---
14.15 - 17.30	Workshops
17.35	Return to hotels by buses
18.35	Transfer from Holiday Inn to reception by bus
18.45	Transfer from hotel Schatten to reception by bus
19.30	Reception by the Mayor of Stuttgart, Prof. Bruckmann (Rathaus-Casino in the town hall of Stuttgart)
approx. 22.00	Buses returning to hotels

THURSDAY, OCTOBER 29TH 1987:

8.25	Transfer from Holiday Inn to MPI by bus
8.35	Transfer from hotel Schatten to MPI by bus
9.00 - 12.30	Workshops
12.30 - 14.15	--- Luncheon ---
	Core Member Meeting (hotel Schatten):
12.35	Departure for hotel Schatten by bus
14.00	Return from hotel Schatten by bus
14.15 - 17.30	Workshops
17.35	Return to hotels by buses
18.25	Transfer from hotel Schatten to Remstal by bus
18.40	Transfer from Holiday Inn to Remstal by bus
19.30	Dinner in Endersbach (Rathauskeller), given by the Japanese side (hosted by Prof. Yanai, sponsored by Japanese companies)
approx. 23.00	Buses returning to hotels

FRIDAY, OCTOBER 30TH 1987:

8.25	Transfer from Holiday Inn to MPI by bus
8.35	Transfer from hotel Schatten to MPI by bus
	(1) Summary Reports from the Workshops
9.00 - 9.25	New Media
9.25 - 9.50	Computer
9.50 - 10.15	Semiconductors
10.15 - 10.30	(2) Closing Remarks Prof.Dr. Yanai Prof.Dr. Engl Mr. Atarashi, MITI Mr. Thomas, BMFT
	(3) Technical Visits
10.40	Departure of the buses for technical visits Technical visits incl. luncheon
14.15	Return from technical visits to hotels or MPI by buses
15.00	Check-out from hotels and departure or Continuation to Munich

Munich:

19.30 Reception by the Bavarian Government, represented by Dr. Stoiber, Minister of State, for the participants of the 6th German-Japanese Forum on Communication Science and of the 4th Germany-Japan Forum on Information Technology

II. New Media Workshop

WEDNESDAY, OCTOBER 28TH (AFTERNOON):

14.15 - 14.45	Introduction by the chairmen (Prof.Dr. Baack, HHI and Prof.Dr. Okoshi, University of Tokyo)
	1st topic: HDTV-Displays **(Co-chairmen: Prof.Dr. Mahler, HHI and Mr. Sawabe, NHK)**
14.45 - 15.10	Low and High Voltage Thin Film Transistors for Adressing Flat Panel Displays (Prof.Dr. Lüder, University of Stuttgart)
15.10 - 15.35	A Large Full-Color Flat Panel Display for HDTV (Mr. Hirashima, NHK)
15.35 - 16.00	Materials for Color TV Based on Liquid Crystal Technology (Dr. Felcht, Hoechst)
16.00 - 16.40	--- Coffee break ---
16.40 - 17.05	Flat CRT Panels (Mr. Nonomura, Matsushita Electric)
17.05 - 17.30	Solid State Light Valves (Dr. Gerhard-Multhaupt, HHI)

THURSDAY, OCTOBER 29TH (MORNING):

9.00 - 9.50	Discussion on HDTV Flat Panels and Projectors for Home Application
	2nd topic: HDTV Transmission (Co-chairmen: MR Steiner, BMP and Dr. Toda, NTT)
9.50 - 10.15	HDTV Transmission in Telecommunications (Dr. Miki, NTT)
10.15 - 10.40	Review of Proposals for HDTV Transmission (Dr. Stenger, Research Institute of DBP)
10.40 - 11.10	Discussion on HDTV Transmission
11.10 - 11.30	--- Coffee break ---
	3rd topic: HDTV Studio Equipment (Co-chairmen: Dr. Wilkens, IRT and Prof.Dr. Tsujii, Tokyo Institute of Technology)
11.30 - 11.55	Progress in HDTV Recording Technologies (Mr. Hashimoto, Sony)
11.55 - 12.05	Remarks on State of the Art in HDTV Recording Technologies (Dr. Hausdörfer, BTS)
12.05 - 12.30	Discussion on HDTV Recording Technologies

THURSDAY, OCTOBER 29TH (AFTERNOON):

14.15 - 14.40	Pickup Tube or Solid State Imager - Alternatives for HDTV Image Signal Generation (Dr. Hausdörfer, BTS)
14.40 - 15.05	Progress in HDTV Camera Equipment (Mr. Hori, Ikegami Tsushinki)
15.05 - 15.35	Discussion on HDTV Camera Technologies
15.35 - 15.55	--- Coffee break ---

4th topic: Three-Dimensional Television (Co-chairmen: Dr. Wilkens, IRT and Prof.Dr. Tsujii, Tokyo Insitute of Technology)

15.55 - 16.20	Autostereoscopic Three-Dimensional Television Experiment Using Lenticular Sheets and a High-Resolution Braun Tube (Prof.Dr. Hamasaki, University of Tokyo)
16.20 - 16.45	3DTV without Glasses (Mr. Börner, HHI)
16.45 - 17.10	Discussion on Three-Dimensional Television
17.10 - 17.30	Concluding Remarks by the chairmen (Prof.Dr. Okoshi, University of Tokyo and Prof.Dr. Baack, HHI)

III. Computer Workshop

WEDNESDAY, OCTOBER 28TH (AFTERNOON):

1st topic: Fault-Tolerant Systems

14.15 - 14.45 Data Base Architecture
(Prof.Dr. Leilich, University of Braunschweig)

14.45 - 15.30 Research Activities on Fault-Tolerant Systems in Japan
(Prof.Dr. Tohma, Tokyo Institute of Technology)

15.30 - 15.45 --- Coffee break ---

15.45 - 16.30 Realization of Fault-Tolerance
-Autonomous Decentralized System-
(Dr. Ihara, Hitachi)

16.30 - 17.00 Fault-Tolerance by Synchronisation of Real-Time Task Systems on Multiprocessor Duplex Computers
(Dr. Meyerhoff, Krupp Atlas Elektronik)

17.00 - 17.30 DELTA-4: The European Research Project for an Open, Fault-Tolerant Multicomputer Architecture
(Dr. Behr, GMD)

THURSDAY, OCTOBER 29TH (MORNING):

2nd topic: Software Engineering Methodology

9.00 - 9.45 Rapid Innovation in Industrial Automation, a Challenge for Software Engineering
(Mr. Howein, Siemens)

9.45 - 10.30 Research and Development Trends on Automating the Software Production in Japan
(Dr. Hanata, NTT)

10.30 - 11.00 --- Coffee break ---

11.00 - 11.45 An Overview of Software Engineering Architecture/One (SEA/I)
(Mr. Matsumoto, NEC)

11.45 - 12.30 Framework Approach to Integrated Tool Sets for Software Engineering
(Prof.Dr. Steusloff, FhG)

THURSDAY, OCTOBER 29TH (AFTERNOON):

3rd topic: Software Engineering Environments

14.15 - 14.45 The Evolution in Structured Methodologies Achievements in Methods and Tools
(Dr. Hruschka, GEI)

14.45 - 15.15 Database Support for Software Engineering Environments
(Dr. Dittrich, FZI)

15.15 - 16.00 SIGMA (Software Industrialized Generator and Maintenance Aids) System and Workstations
(Mr. Akima, IPA)

16.00 - 16.15 --- Coffee break ---

16.15 - 17.00 Overview of Sigma Multi-Media Window System (Sigma MMW)
(Mr. Akima, IPA)

17.00 - 17.30 The Joint Venture Project "EUREKA Software Factory"
(Mr. Abbenhardt, Softlab)

IV. Semiconductor Workshop

WEDNESDAY, OCTOBER 28TH (AFTERNOON):

Opening by the chairmen

14.15 - 15.00 Two-Dimensional Electron Systems in Compound Semiconductors (Prof.Dr. Pilkuhn, University of Stuttgart)

15.00 - 15.45 Al GaAs/GaAs Quantum Well Laser for OEIC Application (Dr. Sakurai, Fujitsu)

15.45 - 16.00 --- Coffee break ---

16.00 - 16.45 Characterization of Semiconductor Crystals Using Synchroton Radiation (Dr. Matsui, NEC)

16.45 - 17.30 High Resolution Optical Analysis of Defects in Semiconductors (Dr. Weber, MPI)

THURSDAY, OCTOBER 29TH (MORNING):

9.00 - 9.45 Analysis of Oxygen in Silicon (Dr. Wagner, Wacker-Heliotronic)

9.45 - 10.30 Wafer Design for Silicon Devices (Dr. Takasu, Toshiba Ceramics)

10.30 - 11.00 --- Coffee break ---

11.00 - 11.45 High Resolution Electron Microscopy of Microelectronics Devices
(Dr. Föll and Dr. Oppolzer, Siemens)

11.45 - 12.30 High Resolution Observation of Fine Structure in Compound Semiconductors Using TEM, SEM, μ-RHEED and STM
(Dr. Ogirima, Hitachi)

THURSDAY, OCTOBER 29TH (AFTERNOON):

14.15 - 15.00 Electron Spin Resonance Observation of Defects in Device Oxides
(Prof.Dr. Sugano, University of Tokyo)

15.00 - 15.45 The Physics of Gettering in Semiconductors
(Dr. Graff, TEG)

15.45 - 16.00 --- Coffee break ---

16.00 - 16.45 Concept and Basic Technologies for 3-D IC Structures
(Dr. Akasaka, Mitsubishi)

16.45 - 17.30 Resist Technology for Submicron Lithography
(Dr. Buhr, Hoechst-Kalle)

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10. 企　業　訪　問

10. 企 業 訪 問

Technical Visits

Tour 1: Research and Development in Büsnau

Tour 2: Standard Elektrik Lorenz AG (SEL)

Tour 3: Daimler-Benz AG

Tour 4: Robert Bosch GmbH

Tour 1: Research and Development in Büsnau

Agenda:

10.45 h	Meeting at MPI - foyer
	Guided tour
	o liquid phase epitaxy
	o molecular beam epitaxy
	o photoluminescence
	o time-resolved photoluminescence
11.30 h	Transfer to Institute of Microelectronic
11.40 h	Guided tour
	o Pilot line for integrated circuits
12.20 h	Transfer to Technology Centre
12.30 h	Lunch
13.00 h	Transfer to University of Stuttgart (4. Physikalisches Institut)
13.10 h	Overview on basic research and technology activities on III - V semiconductors
	o Electron-beam lithography
	o Ion implantation
	o Reactive ion etching
14.00 h	Transfer back to MPI

Tour 2: Standard Elektrik Lorenz AG (SEL), Stuttgart

Agenda:

10.30 h	Bus transfer from MPI to SEL
11.00 h	Welcome and Company presentation
11.15 h	Presentation on System 12
	o Digital Switching System
	o System Architecture Hardware/Software Design ISDN
	o Outlook on the future
11.45 h	Visit to the product exhibition with explanation by experts
	o Switching and transmission products
	o Digital PABX and terminals
	o Railway control system
	o NAVAIDS
in parallel:	
12.15 h	Visit to System 12 integration and test center
	o System 12 Integration
	o ISDN
12.15 h	Visit to laboratory of optical components
13.00 h	Lunch at the SEL casino
14.00 h	Bus transfer back to MPI

Tour 3: DAIMLER-BENZ AG, Sindelfingen

Agenda:

10.45 h	Departure by bus from MPI
11.30 h	Arrival in the Customer Center Greetings and information about the plant
11.45 h	Film "Mercedez-Benz in Sindelfingen"
12.10 h	Factory tour
	o Pressing plant
	o Bodyshell-manufacture
	o Final assembly
13.15 h	Lunch
14.15 h	Return to MPI

Tour 4: Robert Bosch GmbH, Gerlingen

Agenda:

10.30 h	Pick-up at MPI
11.00 h	Introduction into research activities at Bosch
11.30 h	Visit of the research laboratory
	o surface analysis
	o Ta-Ni thin film technology
	o modelling of fuel injection nozzles
	o automatisation of visual inspection in manufacturing
12.30 h	Lunch
14.00 h	Return to MPI
14.30 h	Arrival at MPI

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